Design and Performance Optimization of a Single-Phase Inverter Comparing PID and PR Control



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Declaration

This document was submitted to the Department of Electrical Engineering, Nelson Mandela University, in complete fulfilment of the requirements for a degree in Honours, Electrical Engineering. In accordance with Rule G5.11.4, I hereby declare that the above-mentioned project and research is my own work and that it has not previously been submitted for assessment to another University or for another qualification. All the work herein is my own, and all external sources have been appropriately referenced.

Signature: 

Date: 02 October 2026

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I would like to thank my supervisor, Dr Kumeshan Reddy for his guidance and constructive feedback throughout the course of this project. His expertise and insights have been of great assistance.

Abstract

This document investigates the design and optimization of a single-phase 1kVA pure sine wave inverter, with a focus on output voltage regulation, harmonic reduction and conversion efficiency. Pure sine wave inverters have many advantages over other converters such as operation with very low harmonic distortion, reduction in audible noise and easier running of inductive loads such as pumps and motors.

One of the aspects discussed in this paper is the various methods used to maintain a stable output voltage under varying load conditions. This can be done by implementing a closed-loop control system which uses voltage feedback to regulate the output voltage. In this document a comparison is done between proportional-integral-derivate (PID) and proportional-resonant (PR) control techniques where performance parameters such as transient behaviour and steady-state error are evaluated.

An output LC filter was designed where experimental testing was done by varying the series filter inductance and parallel capacitance to investigate their effects on total harmonic distortion (THD), idle current and efficiency. Certain aspects of the inverter were modelled and simulated before hardware implementation, after which a physical prototype was built and tested. The results were recorded and discussed in order to choose a final optimized inverter design.

The final prototype was a transformer-based inverter which used fast-slow leg unipolar PWM, a 20 kHz switching frequency, closed-loop PI control for voltage regulation and an optimised LC filter. Although the prototype was operated with 1 kVA loads, further continuous full-load testing is required to establish the inverter’s thermal capabilities.

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1. Introduction

1.1. Background

Power electronics first began in 1902 with the invention of the mercury-arc rectifier made by Peter Cooper Hewitt and ever since then, power electronics has been expanding at an incredible rate [1]. In modern times, we know power electronics as the field of electrical engineering concerned with the conversion and control of electrical energy using semiconductor switches [2]. Unlike most electrical systems that mainly rely on passive components or electromechanical switches, power electronic systems use components such as metal-oxide-semiconductor field-effect transistors (MOSFETs), insulated-gate bipolar transistors (IGBTs) and thyristors to control electrical power [2].

Power electronic converters play an essential role in modern electrical energy systems by allowing efficient conversion and control of electrical power. These converters convert electrical energy from one form to another, modifying voltage, current or frequency to efficiently obtain the desired form of electrical energy [1], [2]. There are many types of converters including AC-DC, DC-AC, DC-DC and AC-AC.

DC-AC converters, commonly referred to as inverters, have become increasingly important in many power electronics applications. Inverters are commonly found in renewable energy systems, uninterruptable power supplies, electric vehicles and motor drives [2]. In the renewable energy sector inverters are typically used to convert battery voltage into a conventional utility AC voltage allowing one to use household appliances which require 230V AC, 50Hz in South Africa.

1.2. Problem statement

In the last decade, South Africa's total power generation has failed to meet the local populations demand, driven primarily by aging infrastructure and delays in completing major capacity projects [3]. This resulted in the implementation of loadshedding which is the deliberate, temporary shutdown of electric power in parts of the distribution system when electricity demand is greater than the available supply. In response, some citizens bought backup generators which have many unavoidable limitations such as high maintenance, noise pollution, release of harmful gasses and high operating costs [4]. Operating costs being one of the most notable disadvantages because of the steady rising fuel prices in South Africa.

An alternative to generators would be photovoltaic (PV) systems where a core component required in the system would be the inverter. An inverter has little to no maintenance and operating costs and does not produce noise or air pollution. However, an inverter is only a viable solution when designed well. Traditional design topologies suffer from:

- Lack of robustness
- Excessive power losses
- Poor output waveform quality
- Inability to maintain voltage stability under dynamic load conditions

This project focusses on addressing these limitations by making use of an optimized inverter design to achieve better performance in all areas.

1.3. Aim and Objectives

The overall aim of this project is to design and optimize a 1 kVA single-phase inverter. Additionally, the project aims to identify a suitable combination of control strategy and output-filter configuration for maintaining a stable sinusoidal output with low total harmonic distortion (THD) and acceptable efficiency. For the research aspect of this project, both PID and PR control strategies will be compared, and various output filter configurations will be evaluated. The performance of each configuration will be compared using parameters such as THD, efficiency, controller response and stability.

To achieve the overall aim, the following objectives should be achieved:

1. **Develop and simulate the system.**
   Use simulations to investigate the best PWM strategy, topology and overall design of the system before hardware and software implementation.

2. **Implement, tune and compare PID and PR control.**
   Develop the two control strategies and document their feedback circuit designs, sampling rates, tuning procedures and output limits.

3. **Evaluate various output-filter configurations.**
   Investigate the effects of filter design on THD and efficiency.

4. **Conduct experimental testing with comparisons.**
   Test the inverter under varying load conditions while maintaining consistent hardware and operating conditions during comparisons.

5. **Identify the best design and its limitations.**
   Determine which controller and filter combination provides the best balance of voltage regulation, waveform quality, transient response and efficiency.

1.4. Research questions

The main research question is:

Under identical operating conditions, how does PID and PR voltage-control strategies affect voltage regulation, transient response and overall performance? Additionally, how does the filter design change the inverters performance?

The following are supporting questions:

1. How effectively does PID and PR control maintain a steady-state output voltage of 230 V AC as the load is varied.

2. How do the two control strategies compare in terms of stability, voltage overshoot, voltage dip and settling time following load application and removal?

3. How do changes in output-filter inductance and capacitance affect output waveform quality, idle power consumption and efficiency?

4. What final inverter design has a good balance of voltage stability, power output capability, robustness, waveform quality and efficiency?

5. What trade-offs arise between harmonic reduction, transient response and conversion efficiency when selecting controller parameters and filter configurations?

1.5. Scope Inclusions and Limitations

Inclusions

Design a system prototype with the following requirements:

- Input voltage: 24V DC
- Output voltage: 230V AC, 50Hz
- Power rating: 1kVA
- Waveform type: Pure sine wave

Research, analysis and documentation:

- Compare PID and PR control strategies for voltage regulation.
- Optimize the output LC filter by testing various configurations.
- Analyse how the changes above affect overall system performance.

Figures and power flow diagrams in this document were created by the author using drawing software, unless they are otherwise cited and referenced.

Limitations

Grid connection, grid synchronization, three-phase operation and battery charging are outside the scope of the project. The direct comparison of results between both PID and PR controllers are limited because both control strategies will require different sample rates, controller gains, feedback circuits and signal conditioning. These differences are considered when analysing the results.

Experimental testing is limited to the loads and instruments available during the project. It will not be possible to assess every type of household appliance or load power factor and testing outside the specified output-power range is not included. The accuracy of the results is affected by instrument accuracy and available hardware at the time.

Simulation models will simplify transformer behaviour such as core losses, copper losses and leakage inductance. The simulations also simplify semiconductor switching behaviour, conductor resistance, voltage drops and source impedances.

The 1 kVA rating represents the design target. The actual output power rating and operating duration are found by experimental testing. Short-duration load tests do not mean the inverter has continuous thermal capability.

2. Literature Review

2.1. Inverter Topologies

Single-phase inverter topologies can be classified based on the semiconductor switch arrangement, transformer configuration and number of power conversion stages [5]. Many designs have been developed over the years with the primary objective being to create high power AC from low voltage DC sources with minimal power losses during the process. In this section we will be reviewing the various design techniques used over the years to achieve this objective.

One way to classify inverters is by their switch configuration:

- Push-Pull
- Half-Bridge
- Full-Bridge

The half-bridge configuration will not be reviewed as it is not commonly used in modern inverters due to its lower power handling capabilities and shortcomings compared to the full-bridge configuration [6].

Another way to classify inverters is by their transformer configuration:

- Transformer-based (low frequency)
- Transformer-less (high frequency)

Most solar inverters do the same basic job, which is converting DC battery power into an AC output more suitable for household loads. However, there are differences in how that conversion process happens which will be discussed.

2.1.1. Push-Pull:

The push-pull configuration is a switching arrangement used in low-voltage power conversion systems and can be commonly seen in older line-interactive UPS designs [7]. A pulse-width-modulation (PWM) controller turns on and off two complementary switches in an alternating sequence. When the top switch is turned on (bottom switch off) current flows through the first half of the transformers centre-tapped primary winding and then when the bottom switch is turned on (top switch off) current flows through the second half in the opposite direction [8]. The alternating magnetic flux in the transformer induces a stepped-up AC waveform in the secondary winding [7], [9].

One advantage of the push-pull design is that it allows the use of a comparatively low number of semiconductor switches compared to other designs [8]. However, it does require a centre-tapped transformer which is not cheap to manufacture. A major problem with the push-pull approach is that the current in the transformer is very suddenly reversed into the opposite direction. This can lead to a reduction in efficiency as well as potential for large voltage spikes [8]. The push-pull arrangement is mostly used for older square wave and modified square wave inverters where the output waveform quality is not as important [8].

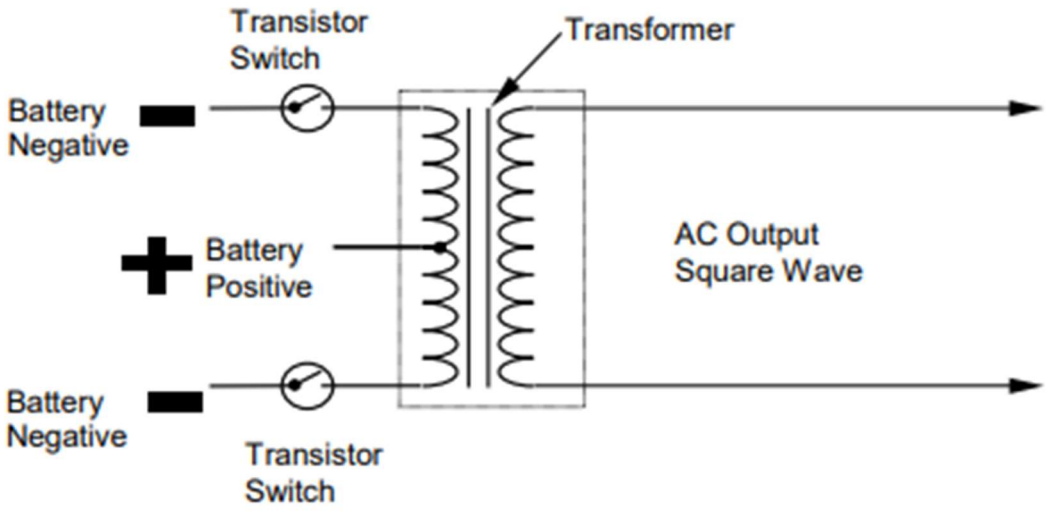


Figure 1: Push-pull topology [8]

2.1.2. Full-Bridge:

The full-bridge inverter, also referred to as the H-bridge inverter, makes use of four semiconductor switches arranged in two switching legs. These switches are turned on and off in complimentary patterns to produce alternating current across the load or transformer primary [5]. The top left and bottom right switches are switched on while the other two stay off, then the top right and bottom left switches are turned on while the other two are kept off. This alternates the direction of current flow from the DC source typically resulting in a modified square wave or sine wave AC output [8].

One very important aspect to remember for the full-bridge inverter is the implementation of a small deadtime between switches in the same leg. If both switches are turned on at the same time, we get ***shoot-through*** which is essentially shorting the DC source across the H-bridge. The full-bridge design efficiency depends mostly upon the quality of the semiconductor switches used and the number of them in parallel [8]. Most of the power losses in this design take place in the switches and the transformer if one is used. This means that as MOSFETs and IGBTs improve over the coming years, the performance of full-bridge inverters will improve too [8].

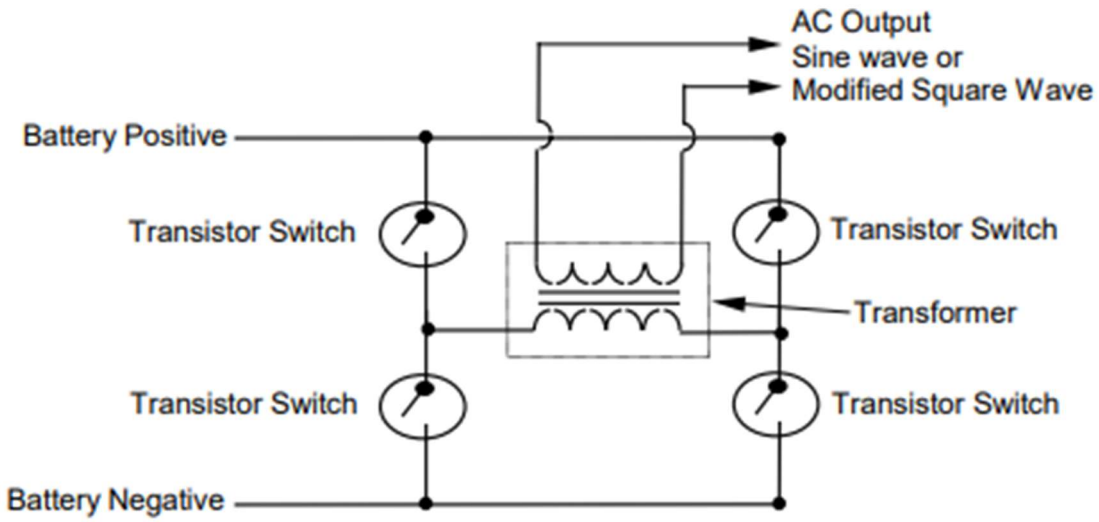


Figure 2: Full-bridge or H-bridge topology [8]

2.1.3. Transformer based inverters

A transformer-based inverter, also referred to as a **low frequency inverter**, switches the DC battery voltage into a low voltage chopped AC waveform. It does this by using a PWM controlled H-bridge which is typically switching somewhere between 10-30kHz [10]. That low voltage AC is then fed into the primary of a large **low frequency transformer** which steps up the voltage to 230V or 120V depending on the intended region. The leakage inductance of the transformer helps filter out a lot of the high frequency switching but additional low pass filtering will be implemented before and after the transformer in order to get a clean sine wave output with minimal harmonic distortion [10], [11].

The large heavy low frequency transformer needed in this design comes with both advantages and disadvantages. It inherently gives the design higher surge capability, meaning starting loads such as pumps, motors and compressors won't be a problem [10]. It also provides galvanic isolation between the circuitry and the AC output resulting in a more robust and safe system. The downside is that these transformers often come with high core and copper-losses resulting in lower overall efficiency as well as a higher idle power draw [10]. One can often find toroidal transformers in these inverters because they typically have better efficiency than traditional EI (laminated square) core transformers [12].

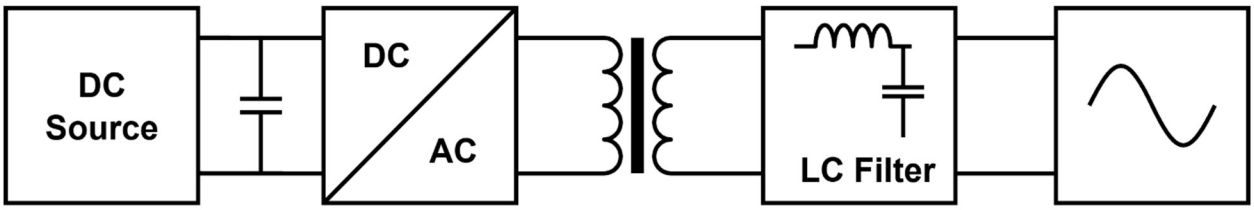


Figure 3: Transformer based inverter (DC-AC-AC)

2.1.4. Transformer-less inverters

A transformer-less inverter, commonly referred to as a high frequency inverter, leaves out the low frequency transformer. Instead, it first makes use of an initial DC-DC boost stage where the battery voltage is stepped up to approximately 325-400V DC using a high-frequency switching converter [10]. This higher voltage DC is then inverted straight into a high-frequency chopped AC voltage via an H-bridge. Once this AC waveform goes through a low pass filter the result is a low THD mains voltage AC sine wave. One aspect that often confuses people is that these "transformer-less" inverters do sometimes use transformers, but they are small high-frequency transformers used in the DC-DC boost stage [13].

Transformer-less inverters do not possess the same high surge power ratings and galvanic isolation that transformer-based inverters do [13]. They struggle to power motors, pumps and compressors which are close their rated power [10]. However, they typically do beat transformer-based inverters in overall efficiency, have lower idle power consumption and are cheaper to manufacture [10]. With that being said, these inverters are better suited for electronics and resistive loads. Another perk of these inverters is that the voltage control loop can feedback into the DC-DC boost converter stage for voltage regulation giving it a quicker response when compared to controlling the switching of the DC-AC stage [13].

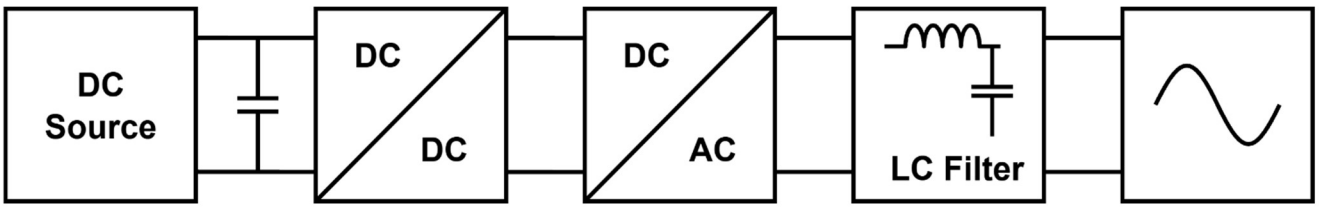


Figure 4: Transformer-less inverter (DC-DC-AC)

2.2. PWM Techniques for Full-Bridge Inverters

2.2.1. Bipolar PWM

Bipolar PWM is arguably the simplest modulation scheme for full-bridge inverters where one leg is controlled with sinusoidal PWM, and the other leg with opposite PWM signals of that leg. Therefore, the output voltage will swing between +Vdc and -Vdc without ever resting at a zero-voltage level [14]. Bipolar PWM works by comparing a reference sine wave (fundamental frequency) with a high-frequency carrier wave to control the switching states of an inverter [15].

One advantage of bipolar PWM is that it is perfectly symmetrical even after the addition of a deadtime and allows the use of only two PWM output pins on a microcontroller. However, bipolar PWM tends to produce more harmonics around multiples of the switching frequency [16]. Because it lacks a zero-voltage state, it typically results in a higher THD at lower modulation indices compared to unipolar PWM. Bipolar PWM also has a high rate of change in voltage (dv/dt) leading to more electromagnetic interference (EMI). It also commonly requires a larger filter such as an LCL filter due to both bridge legs producing high frequency switching harmonics [17].

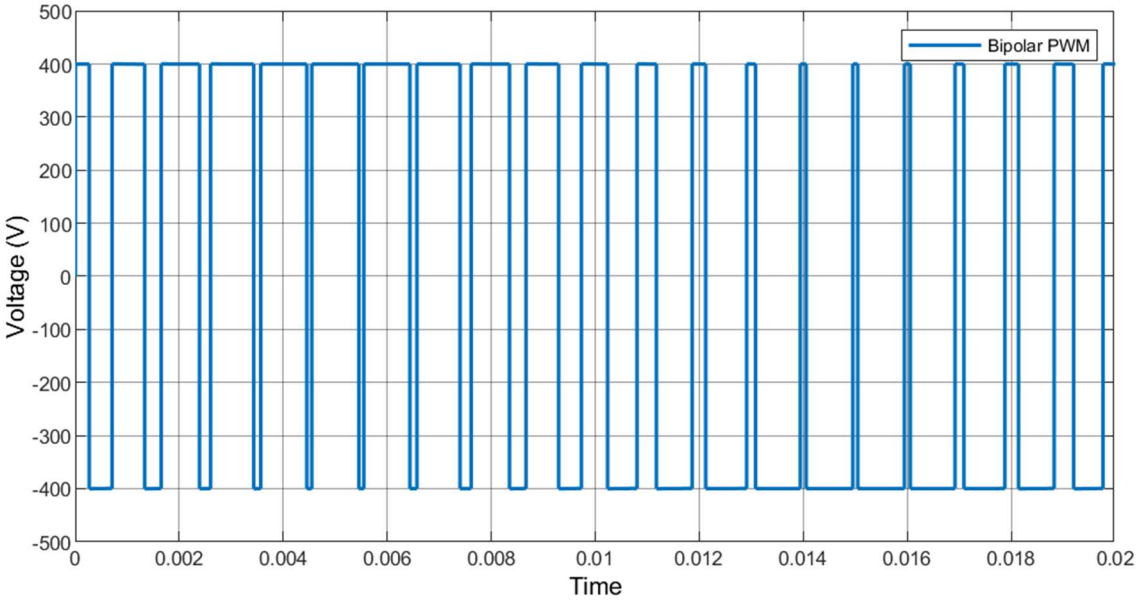


Figure 5: Bipolar PWM (Simulink screenshot)

2.2.2. Standard Unipolar PWM

Standard Unipolar PWM differs from bipolar PWM in that the **output voltage actually reaches a zero-voltage level** so there are now three voltage levels in total (+Vdc, 0, -Vdc) [16]. This method uses two sinusoidal reference waveforms which are 180° out of phase compared against the same carrier waveform. Both legs are switched at a high frequency where leg A is controlled by comparing the original sine wave with the triangular carrier and leg B is controlled by comparing the inverted reference sine wave with the same carrier wave [14].

One major advantage of Unipolar SPWM is the **reduced stress on the switching devices** because the voltage does not swing between the positive and negative extremes [16]. This reduced stress can lead to increased efficiency and possibly longer semiconductor lifespans [17]. Unipolar PWM also results in a more consistent THD reduction across the entire modulation spectrum (0-1) whereas bipolar PWM only has less harmonic distortion when the modulation index is closer to 1 [17] [16].

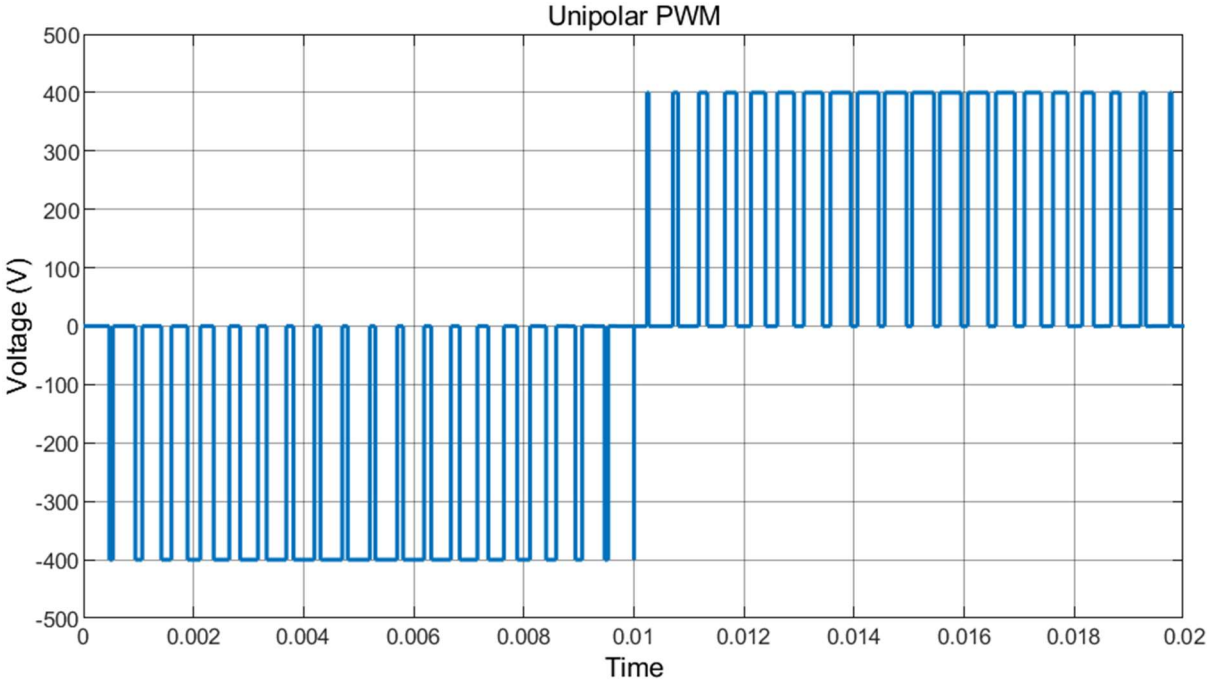


Figure 6: Unipolar PWM (Simulink screenshot)

2.2.3. Fast-Slow Leg Unipolar PWM

The Fast-Slow Leg PWM technique has one leg switching at the switching frequency and the other leg switching at the fundamental frequency (50Hz in our case). Since **only one leg switches at a high frequency**, the switching losses can essentially be halved compared to standard unipolar PWM [14]. This PWM technique induces most of its harmonics at around twice the carrier frequency which benefits inverter designs massively because it allows the use of smaller output filter components to attenuate these unwanted harmonics [18].

As can be seen in the figure below, S1 and S3 gates are controlled by the same PWM signal running at a high switching frequency, except the S3 gate signal is 180° out of phase with S1's gate signal. S2 and S4 gates are controlled by a 50Hz PWM signal with one being 180° out of phase with the other. On the next page, you can find the scoped gate signals for the fast and slow leg. To simplify it, one leg mainly sets polarity while the other leg mainly does the high frequency PWM. An advantage to this is that one could use different (cheaper) semiconductor switches for the slow leg [14]. The main disadvantage to this PWM technique is that it is **prone to zero crossing distortion** after filtering [14].

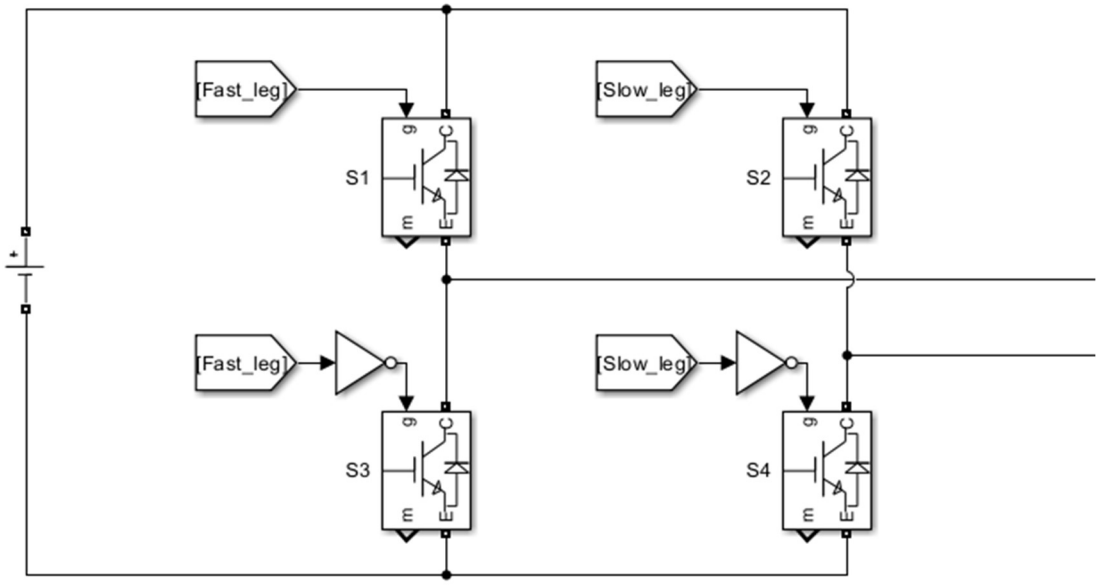


Figure 7: H-bridge setup for fast-slow leg PWM (Simulink screenshot)

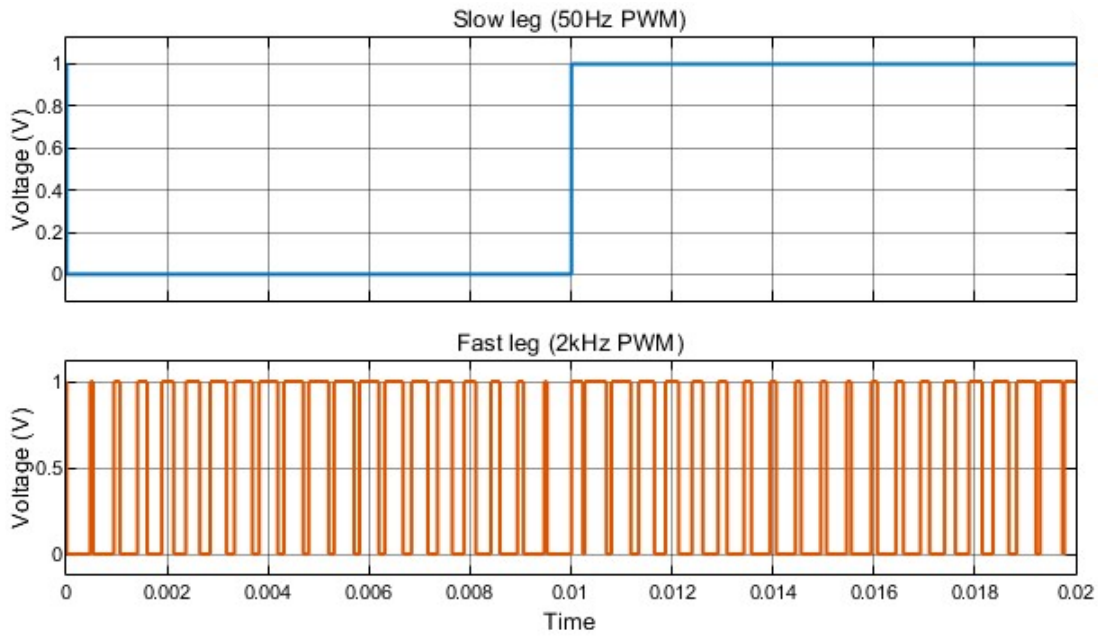


Figure 8: Gate signals for S2 and S1 (Simulink screenshot)

2.2.4. Overall comparison of PWM techniques

The following table was made using information from a referenced article and summarises the full-bridge inverter PWM techniques and their trade-offs [14].

Feature	Bipolar PWM	Standard Unipolar PWM	Fast–Slow Leg Unipolar PWM
Implementation simplicity	Best	Better	Worst
dv/dt stress on semiconductors	Worst	Best	Better
THD (Harmonic distortion)	Worst	Better	Best
Current ripple	Worst	Best	Best
Ripple-related losses	Worst	Best	Best
Switching losses	Worst	Better	Best
Harmonic distribution	Worst	Best	Better
Reverse-direction suitability	Worst	Worse	Best
Sensitivity to zero-crossing distortion	Best	Worse	Worst
Modulation / control complexity	Best	Better	Worst
Thermal stress symmetry between legs	Yes	Yes	No
Cheaper semiconductor for slow leg	No	No	Yes

Table 1: Comparison of PWM techniques for full-bridge inverters [14]

2.3. Control Systems for Inverters

2.3.1. Closed-loop output voltage regulation

In a stand-alone single phase voltage source inverter, the variable we want to control is the voltage supplied to the load rather than the current injected into the grid. Therefore, the control system's main objective is to maintain a stable voltage magnitude and frequency regardless of variations in the DC source and load. This is generally done by measuring the output voltage, feeding it back into the controller which compares it to a reference and adjusts the modulation index based on the calculated error between the measured feedback and the reference [9].

Feedback loops can be put into two categories, which are voltage-only and multiloop structures. The multiloop structure makes use of the measured filter inductor current to improve damping and disturbance rejection [19]. One advantage to multiloop control structures is the ability to implement **short circuit protection**. This is done by monitoring for fault currents and if a fault is found, the controller can immediately switch off all gate drive signals before the fault can cause further damage. However, a multiloop structure with current feedback is more beneficial for grid connected inverters, not standalone designs [9].

An important aspect to consider is the difference between RMS voltage regulation and instantaneous voltage regulation. In instantaneous voltage control, the feedback voltage is compared with a sinusoidal reference throughout the electrical cycle. Instantaneous control can make many error corrections in just one sine wave cycle depending on the speed of the hardware used whereas the speed of the RMS control loop is constrained by the measurements and averaging calculations [9], [19].

2.3.2. Proportional-integral-derivative (PID)

Both PI and PID controllers are the traditional industry standard for DC reference tracking in the synchronous reference frame (dq-frame) [20]. PI controllers are more commonly used in practice due to the derivative term often amplifying noise and causing erratic changes to the system [21]. An ideal PID controller has an infinite gain for tracking DC references where the frequency is zero (ω = 0). The infinite gain is entirely due to the integral (I) action of the controller and results in zero steady state error [21]. The transfer function for an ideal PID controller can be seen below:

$$G_{PID}(s) = K_p + \frac{K_i}{s} + K_d s \tag{1}$$

However, in a practical digital implementation, the derivative action may amplify measurement noise, and the integral action can cause windup. These limitations can be addressed using software implemented derivative filtering, controller output saturation, and integral anti-windup [21].

An ideal derivative controller has a gain that increases proportionally with frequency. This means any high-frequency measurement noise introduced by voltage sensors, analogue to digital converters or any hardware in the feedback circuit can be amplified, resulting in undesirable changes to the controller output. To solve this problem, a first-order low-pass filter can be implemented into the derivative term which limits the controller gain at high frequencies while not affecting the response at lower frequencies [21]. The modified transfer function can be seen below where T_f is the derivative filter time constant.

$$G_{PID}(s) = K_p + \frac{K_i}{s} + \frac{K_d s}{T_f s + 1} \tag{2}$$

2.3.3. Proportional-resonant (PR)

Normally, in a voltage source inverter, the output sinusoidal AC voltage or current signals can be transformed into DC quantities by performing the **Park transform (αβ to dq frame)** [19]. Once this is done a PI controller would be perfectly suitable for tracking the DC reference signal with zero steady state error. However, if we need a controller that can track a sinusoidal reference, a proportional-resonant (PR) controller would be a better solution. An ideal PR controller can track sinusoidal references with zero steady state error [22].

The proportional-resonant controller provides numerous benefits for the control of single-phase inverters, mainly due to its ability to introduce a very high gain at a desired frequency [22]. This results in accurate tracking of sinusoidal references without steady-state error. Unlike a conventional PI controller which is more effectively used in the synchronous reference frame (dq-frame), the PR controller was designed to be a suitable controller in the stationary reference frame (αβ -frame) [22]. An ideal PR controller is designed to provide infinite gain at the selected resonant frequency (ω_o) and the transfer function for it can be seen below:

$$G_{PR}(s) = K_p + \frac{K_r s}{s^2 + \omega_0^2} \tag{3}$$

However, infinite gain can cause stability issues in real-world practical implementations and therefore, a non-ideal PR controller is mostly used instead. A non-ideal PR controller introduces a cutoff frequency or bandwidth (ω_c) around the resonant term (ω_o) [23]. This parameter is called the resonance bandwidth and the transfer function for this non-ideal PR controller can be seen below:

$$G_{PR}(s) = K_p + \frac{2K_r\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \tag{4}$$

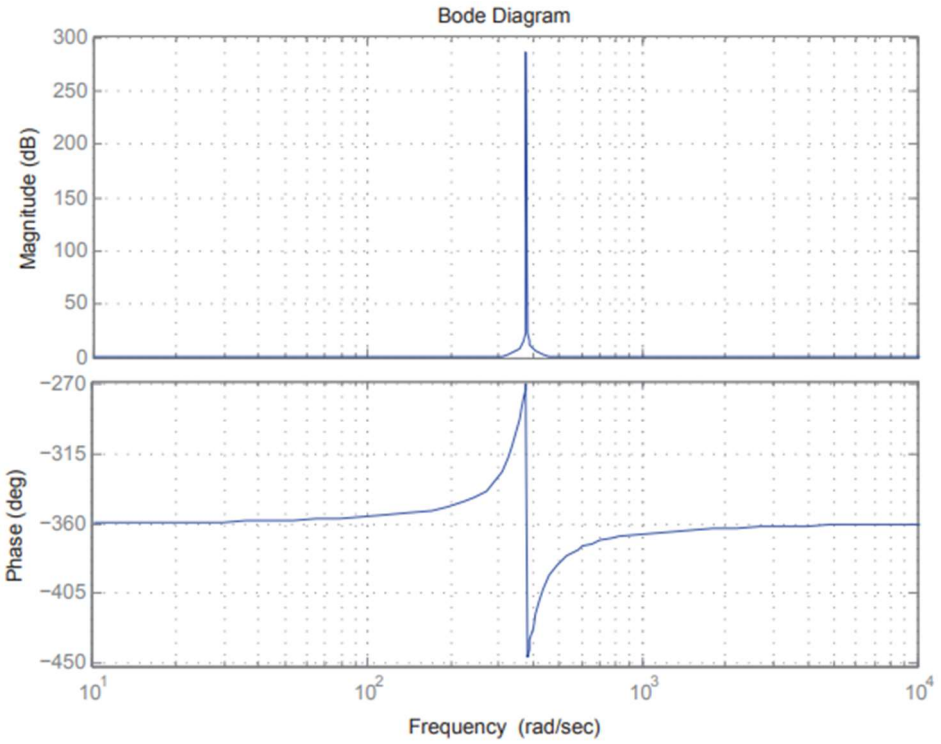


Figure 9: Ideal PR controller [29]

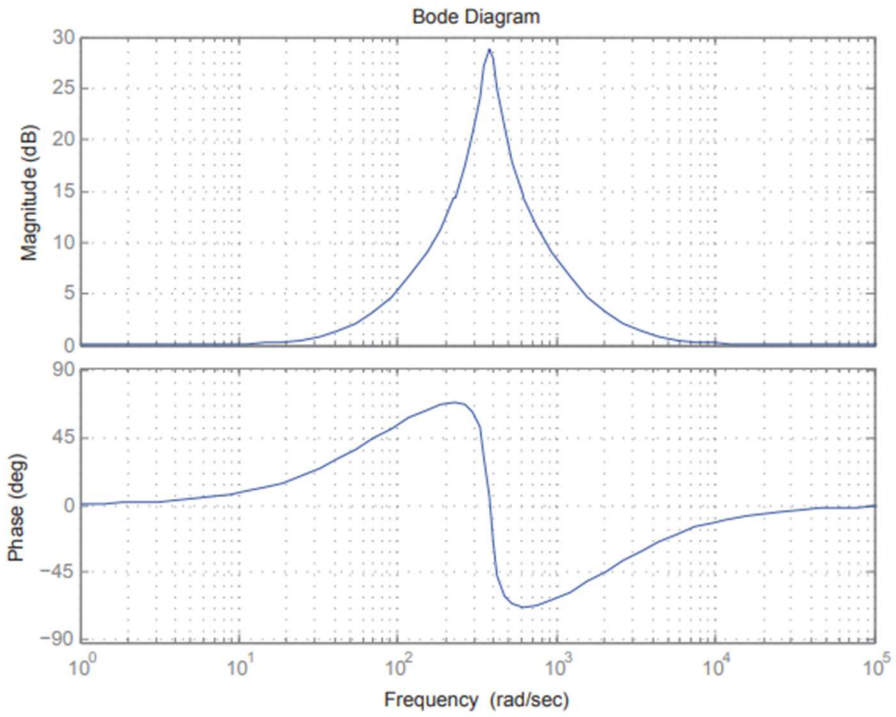


Figure 10: Non-ideal PR controller with a resonant bandwidth [29]

2.4. Output Filtering

A full-bridge inverter still contains high frequency PWM switching ripple which we need to get rid of in order to retrieve the 50Hz fundamental sine wave. A low pass filter is therefore needed to attenuate these unwanted harmonics while retaining the fundamental. However, filter design is not simple as its size, impedance and cost all influence the practical design choice for an inverter [24]. Therefore, proper research and planning need to be done before implementation.

Research shows that for grid-tied inverters an LCL filter is the standard option but for a stand-alone voltage source inverter, the LC filter is a sufficient solution [23]. The series inductor also referred to as the choke opposes high-frequency current ripple, and the parallel capacitor provides a low impedance path to ground for high frequency switching ripple [24]. Many studies state that filter design cannot only be centred around its cut-off frequency, as the load type, physical size, cost and practical availability of components also need to be considered [23] [24] .

The choice of filter size is also directly correlated to the inverters switching frequency. Higher switching frequencies allow for smaller filter components whereas lower switching frequencies require larger filter components to meet THD requirements [24]. Although increased switching frequencies would allow for a smaller LC filter, inductance and capacitance values too high would increase copper and core losses due to skin effect and eddy currents [24]. Typically, engineers will pick a switching frequency between 15-30kHz because these frequencies become inaudible for most human’s hearing and aren’t high enough to cause significant losses [24].

The standard procedure for calculating specific LC filter values includes choosing a practical filter capacitance and a cutoff frequency between the fundamental frequency and the switching frequency. The cutoff frequency should be chosen well below the switching frequency to achieve sufficient attenuation (typically -40 dB/decade), yet high enough above the fundamental frequency (50 Hz) to avoid phase lag or poor dynamic response [25]. The filter inductance can then be calculated by rearranging the following cutoff frequency formula:

$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{5}$$

$$L = \frac{1}{(2\pi f_c)^2 C} \tag{6}$$

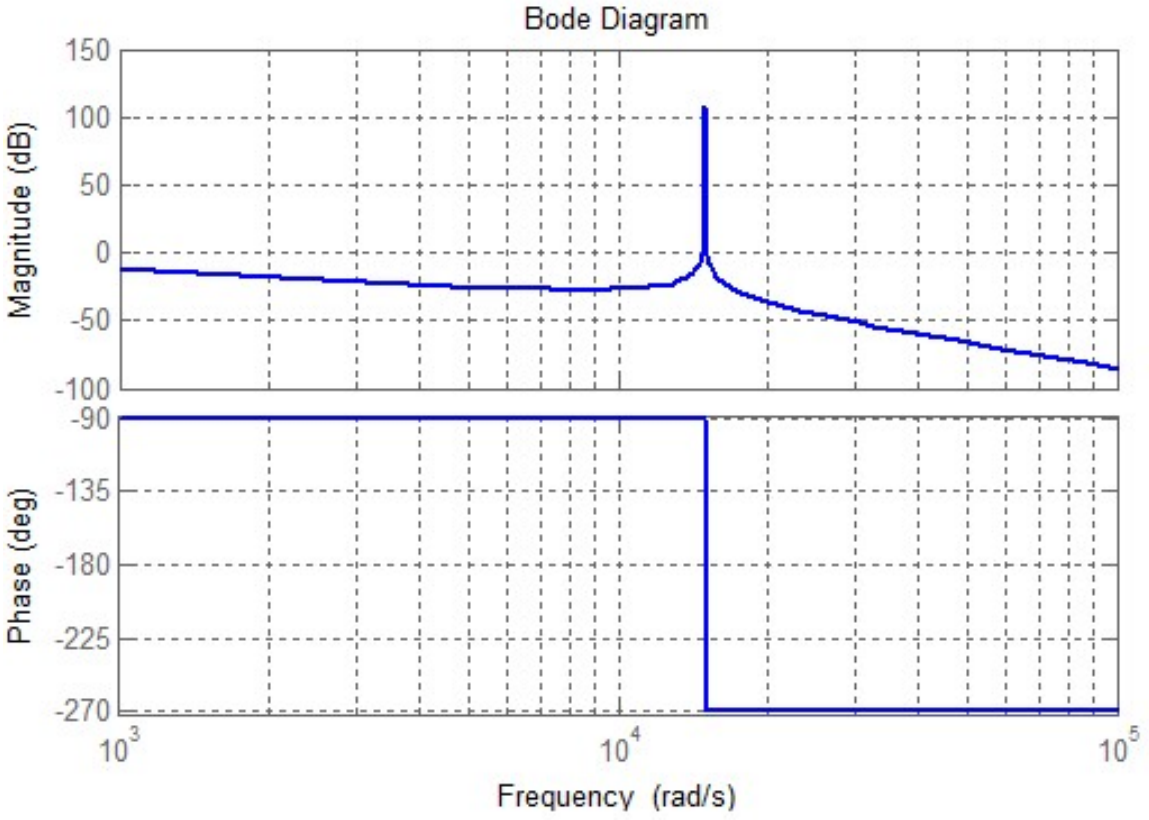


Figure 11: Bode plot for LC filter [30]

3. Simulation and results

This section presents the simulation results obtained from the single-phase inverter model built in MATLAB/Simulink. The simulation was used to compare the performance of two PWM strategies and understand how the proposed closed-loop control systems will work. Bipolar PWM and fast-slow leg unipolar PWM were first compared to determine the most suitable switching technique for practical implementation. After that, PID and PR controllers were designed and tuned to get a better understanding of their working principles before software implementation.

Simulated System Specifications	Value
Power rating	1000W
DC supply	24V
Switching frequency	20kHz
Transformer	14V:230V
Filter inductor (L)	50uH
Filter capacitor (C)	5uF
MOSFET Rds(on)	20mΩ
Bulk DC capacitance	10000uF

Table 2: Simulation specifications

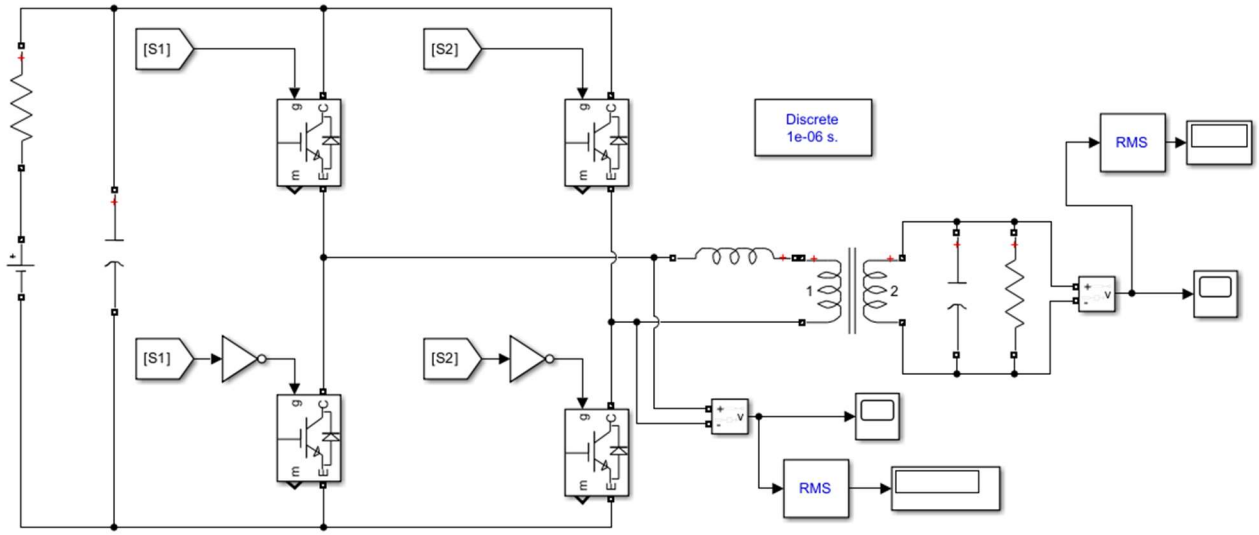


Figure 12: Simulink inverter model

3.1. Bipolar PWM

Figure 13 below shows the output voltage of the H-bridge when operating with bipolar PWM, together with the sinusoidal output waveform after filtering measured at the transformer secondary. One important finding was that **two series chokes were required**, one on each H-bridge output leg in order to fully isolate the high frequency PWM from the low frequency transformer primary via filtering. The efficiency and THD results were recorded.

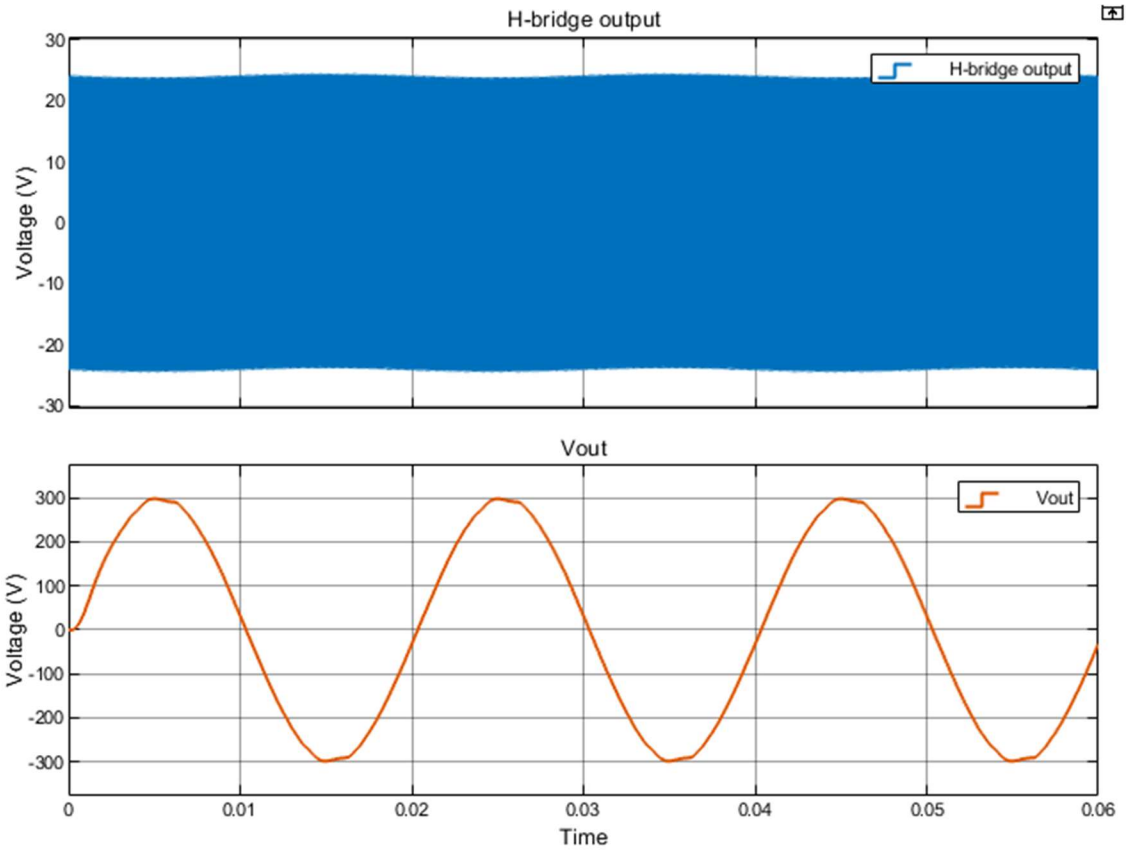


Figure 13: Simulated bipolar PWM

Vin (V)	Iin (A)	Vout (V)	Iout (A)	Efficiency (%)	THD (%)	Load (Ohm)
24	35.54	232.5	2.209	60.21%	0.80%	100
24	50.22	232.5	3.143	60.63	0.78%	80

Table 3: Efficiency and THD results

3.2. Fast Slow Leg Unipolar PWM

Unlike bipolar PWM, only one leg of the H-bridge operates at the 20kHz switching frequency, while the other leg switches at the 50Hz fundamental frequency to set the output polarity. This minimizes the switching losses and also allows the use of a singular choke on the 'fast-leg' of the H-bridge. The results show a major improvement in efficiency and a slight improvement in THD compared to bipolar PWM, which backs up the literature review. Due to these advantages, this is the chosen PWM technique to be used in the prototype.

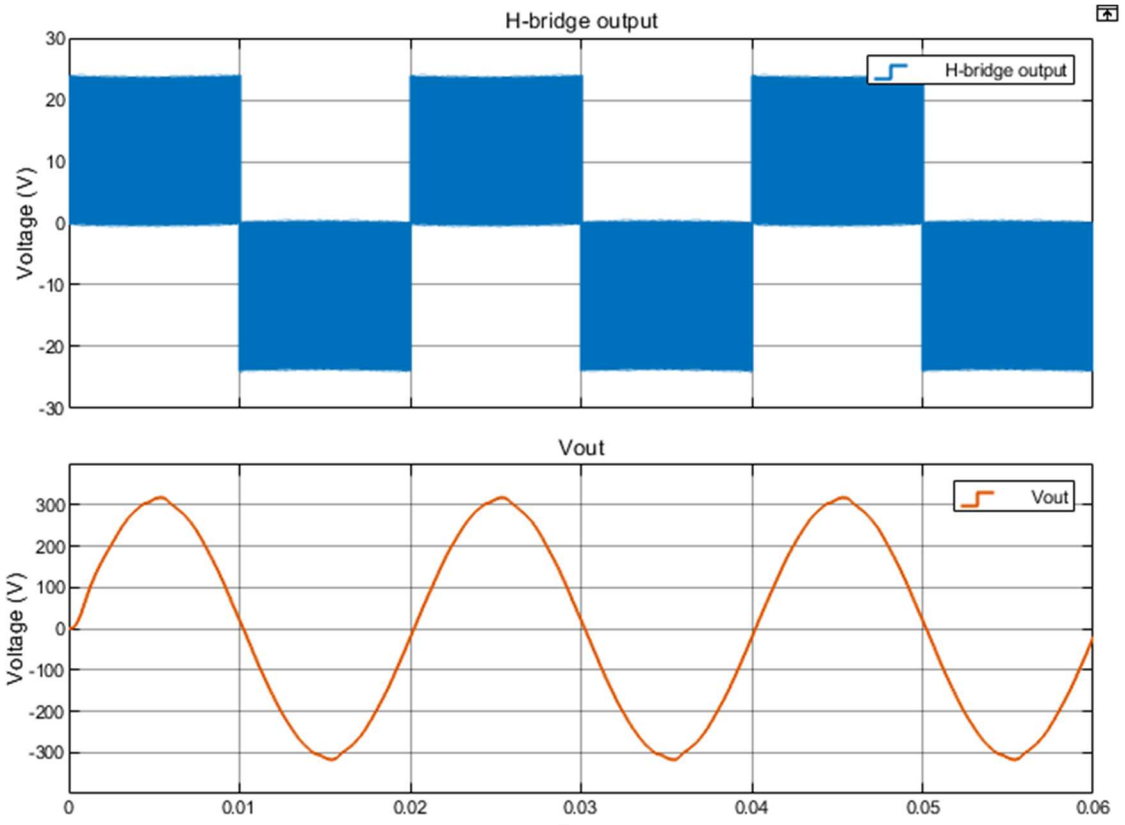


Figure 14: Simulated fast-slow leg PWM

Vin (V)	Iin (A)	Vout (V)	Iout (A)	Efficiency (%)	THD (%)	Load (Ohm)
24	31.62	243.5	2.314	74.25	0.52%	100
24	44.72	243.5	3.292	74.69	0.48%	80

Table 4: Fast-slow leg results

3.3. Comparison of PWM strategies using simulation results

A comparison of the simulation results demonstrates a noticeable performance improvement when fast-slow leg unipolar PWM is implemented instead of bipolar PWM. The efficiency increased from approximately 60.21% to 74.25%, while THD decreased from 0.80% to 0.52% under the simulated operating conditions. The major difference in efficiency is partly because a **high on resistance of 20mΩ was used for the simulated MOSFETs**. This was done on purpose to accentuate the difference in switching losses between the two PWM strategies. The results did end up showing that switching-related power losses are reduced when using fast-slow leg unipolar PWM, improving the overall inverter efficiency.

Another important difference was found in the output filtering requirements. The bipolar configuration required two series chokes, one on each output leg of the H-bridge, to attenuate the high frequency PWM before reaching the transformer. In comparison, fast-slow leg unipolar PWM allowed the implementation of a single series choke. This simplifies the filter design, reduces the number of expensive filter components and potentially reduces the associated copper and core losses. Considering both the efficiency and harmonic performance improvements, fast-slow leg unipolar PWM was selected for the practical inverter prototype.

It should be noted that the output voltages differed between the two configurations which can affect both efficiency and THD measurements. Therefore, the results should be taken as a comparison of the simulated implementations rather than a perfectly controlled comparison of PWM techniques at identical output conditions.

3.4. PID Controller

The following two subsections showcase the design of both the PID and PR controllers instead of directly comparing results. The reason why no results are obtained for the PID and PR controller simulations is because I wanted the comparison to be done after obtaining practical results instead of theoretical ones. However, I did include screenshots of an FFT analysis and THD readings for each controller.

The figure below shows the simulated closed-loop PID control system where the controller output is the modulation index being fed into the plant and the feedback is the measured RMS output voltage. Note that the reference used is a step reference where the value 1 is the equivalent to 230V RMS. The integration method used was trapezoidal integration and anti-windup settings were enabled. The controller was manually tuned, and the final chosen gains were Kp = 0.1, Ki = 1.5 and Kd =0.001. It was found that higher derivate gains than this caused instability and oscillations. The modulation index was also limited between 0 and 1 to prevent over and under modulation.

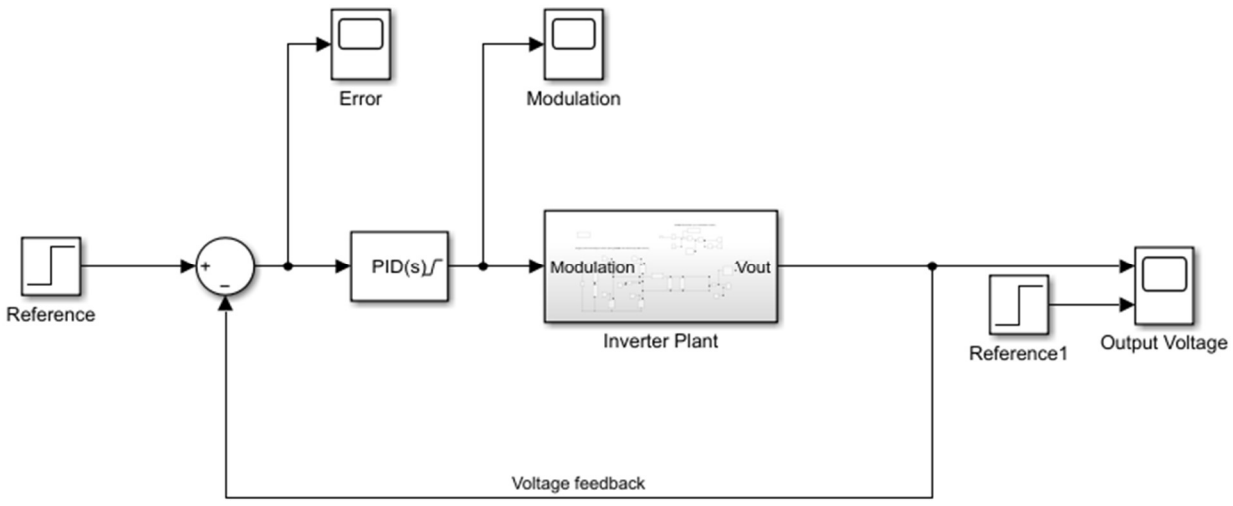


Figure 15: Simulated PID controller

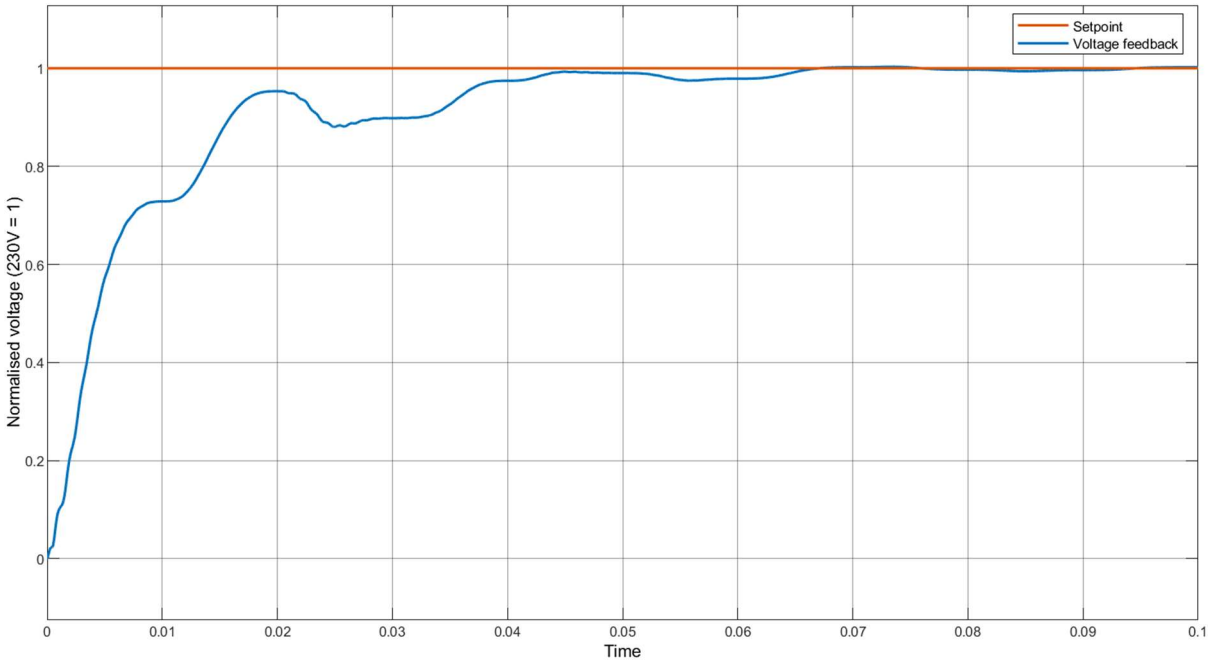


Figure 16: Simulink PID step response

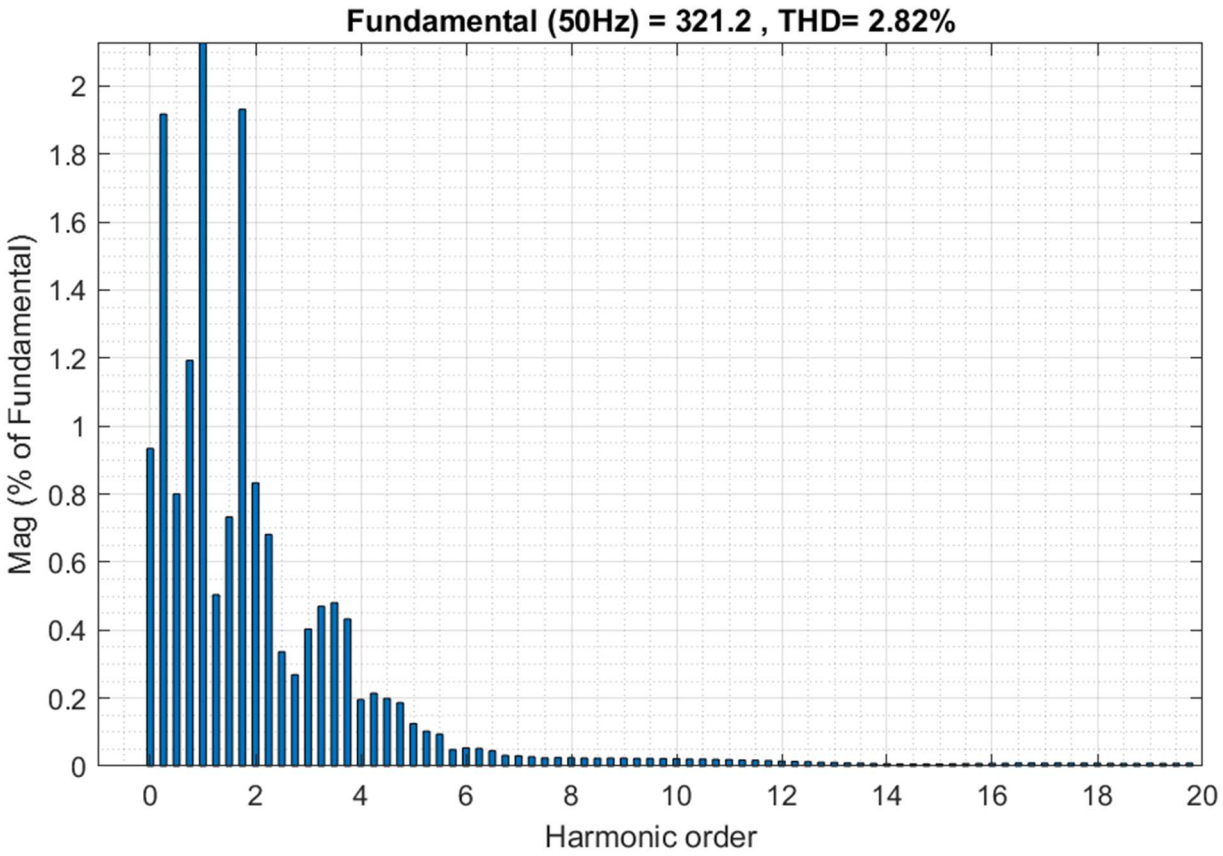


Figure 17: Simulink PID FFT analysis

3.5. PR Controller

Unlike PID the PR controller makes use of a sinusoidal reference with a frequency of 50Hz and an amplitude of 325.26V. The measured instantaneous output voltage is compared with the reference to obtain an error signal, which is then used by the controller to adjust the modulation index. The PR controller that can be seen in the figure below is a non-ideal PR controller which includes a resonant bandwidth of ω_c = 3rad/s. The inclusion of this resonant bandwidth allows the controller to maintain high gain around 50Hz without the theoretical infinite gain of an ideal PR controller. The chosen controller gains were similar to that of the PID simulation Kp = 0.1, Kr = 1.5, ω_c = 3rad/s and ω_o = 2*PI*50.

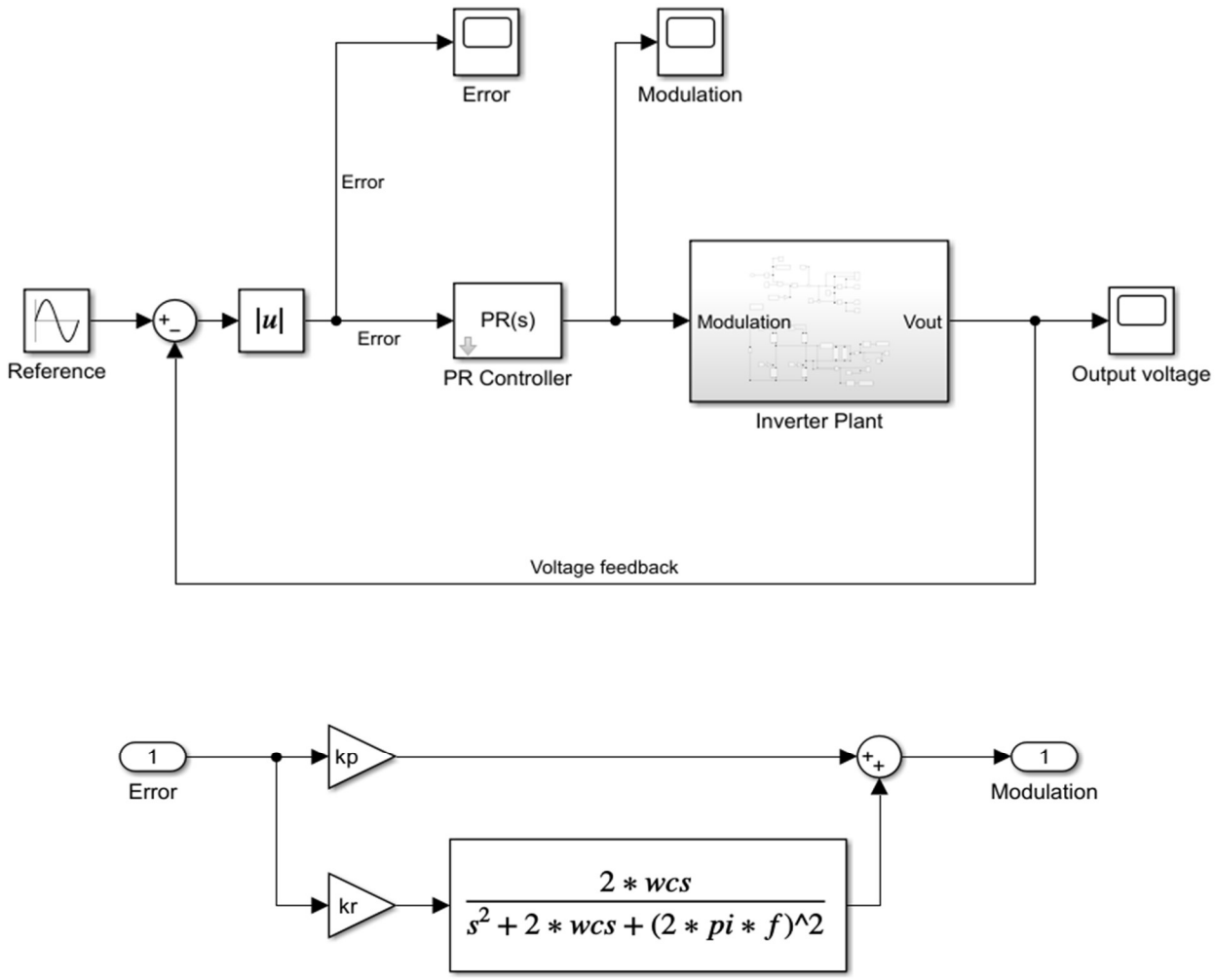


Figure 18: Simulated PR controller

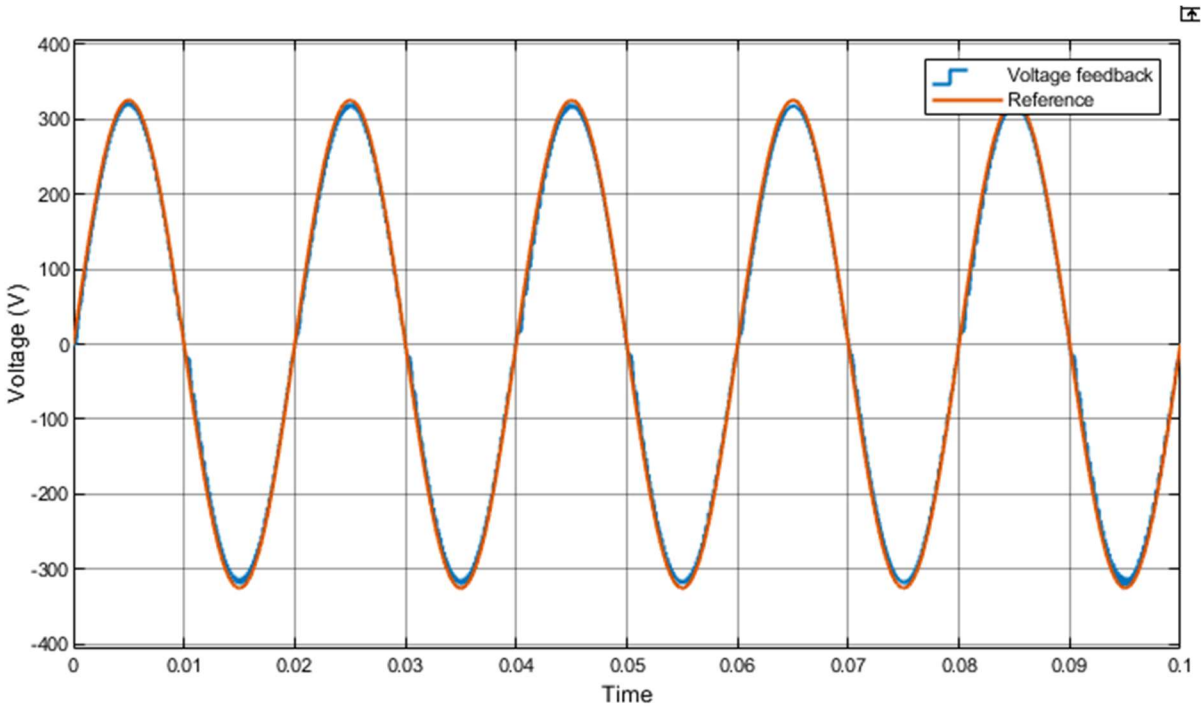


Figure 19: Simulink PR controller reference tracking

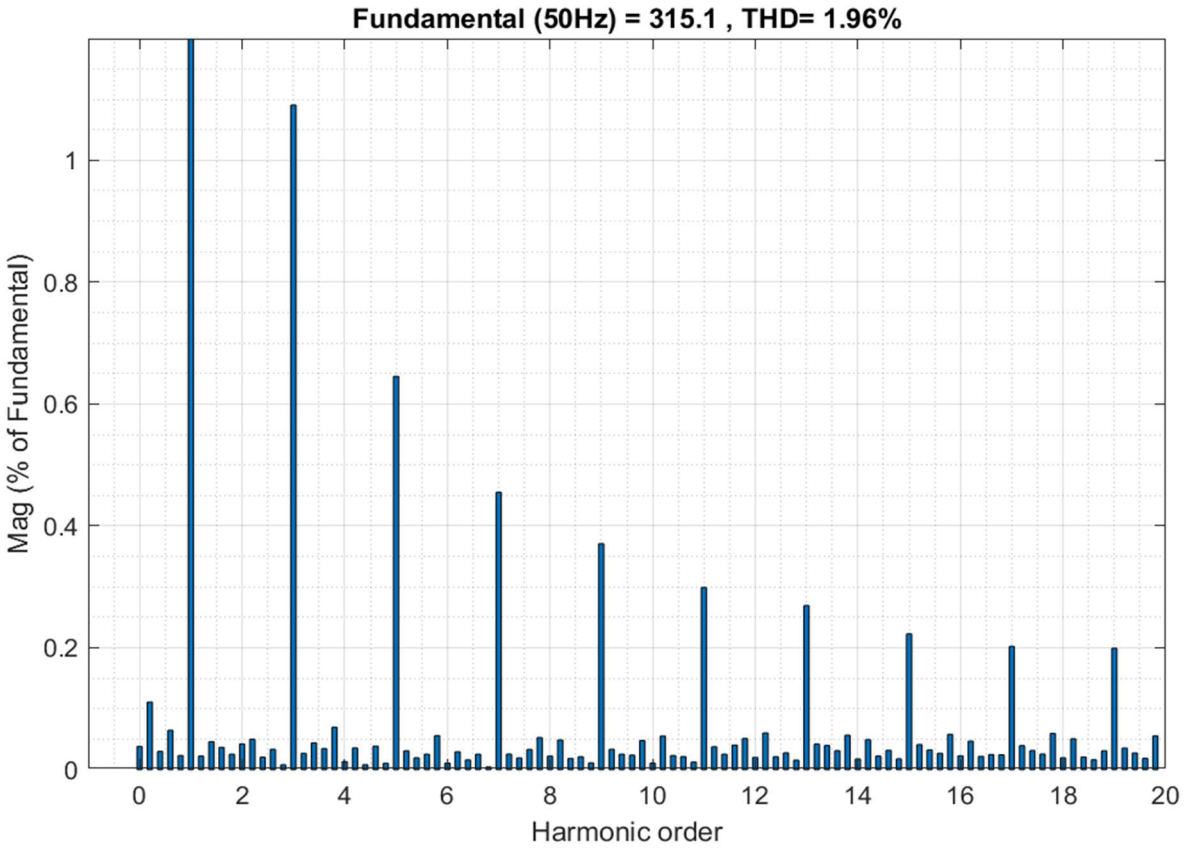


Figure 20: Simulink PR FFT analysis

4. Design and hardware implementation

4.1. PCB Design

The PCB was designed using EasyEDA software and all basic design rules were followed. Both the power section (right side) and control section (left side) were separated to prevent compounding damage should there be a fault. The fast switching digital and sensitive analogue circuitry were also kept separate in order to minimize noise and interference. Enough space was left between traces in order to prevent crosstalk and a continuous copper ground plane was used to give signals a low impedance return path to ground and prevent EMI. Any high voltage sections were labelled with warnings for safety purposes. The PCB was ordered from JLCPCB, and components were soldered once it was delivered.

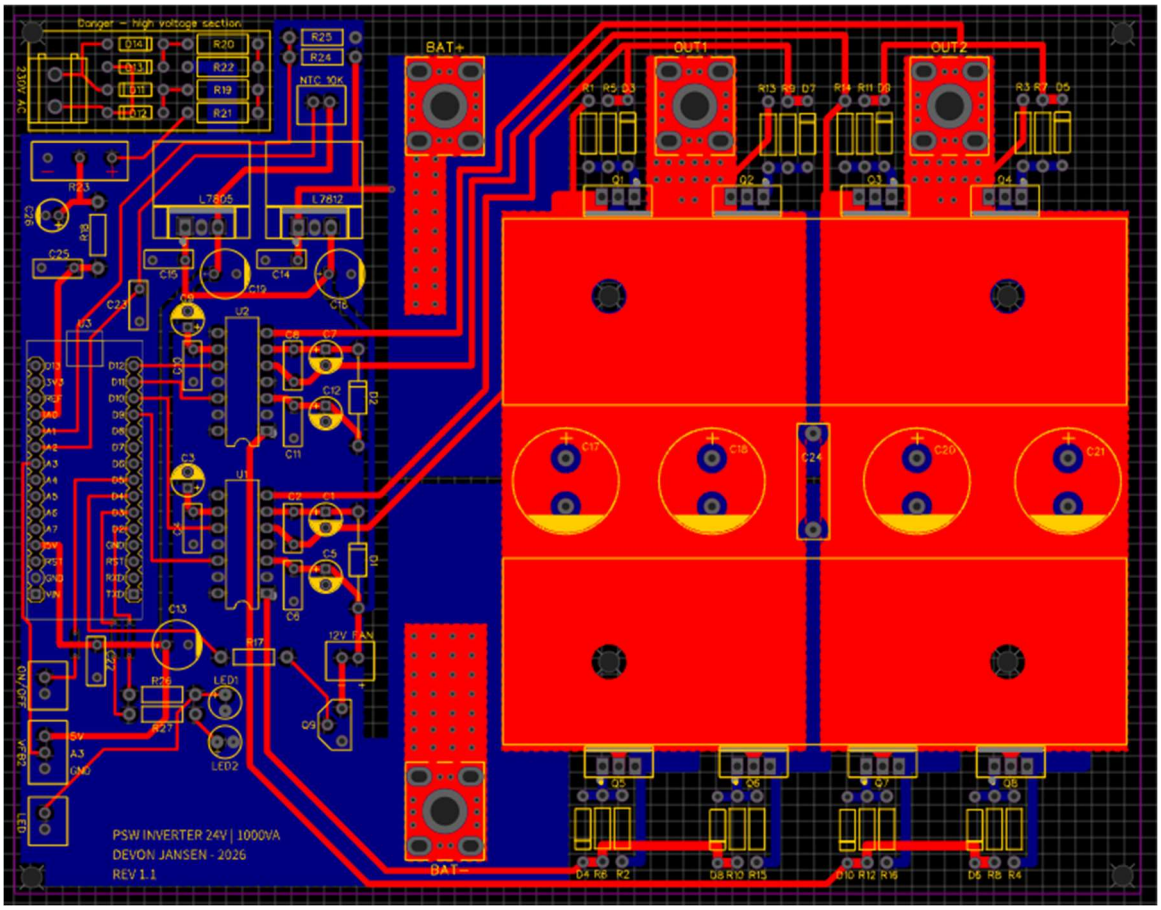


Figure 21: Designing the PCB in EasyEDA software

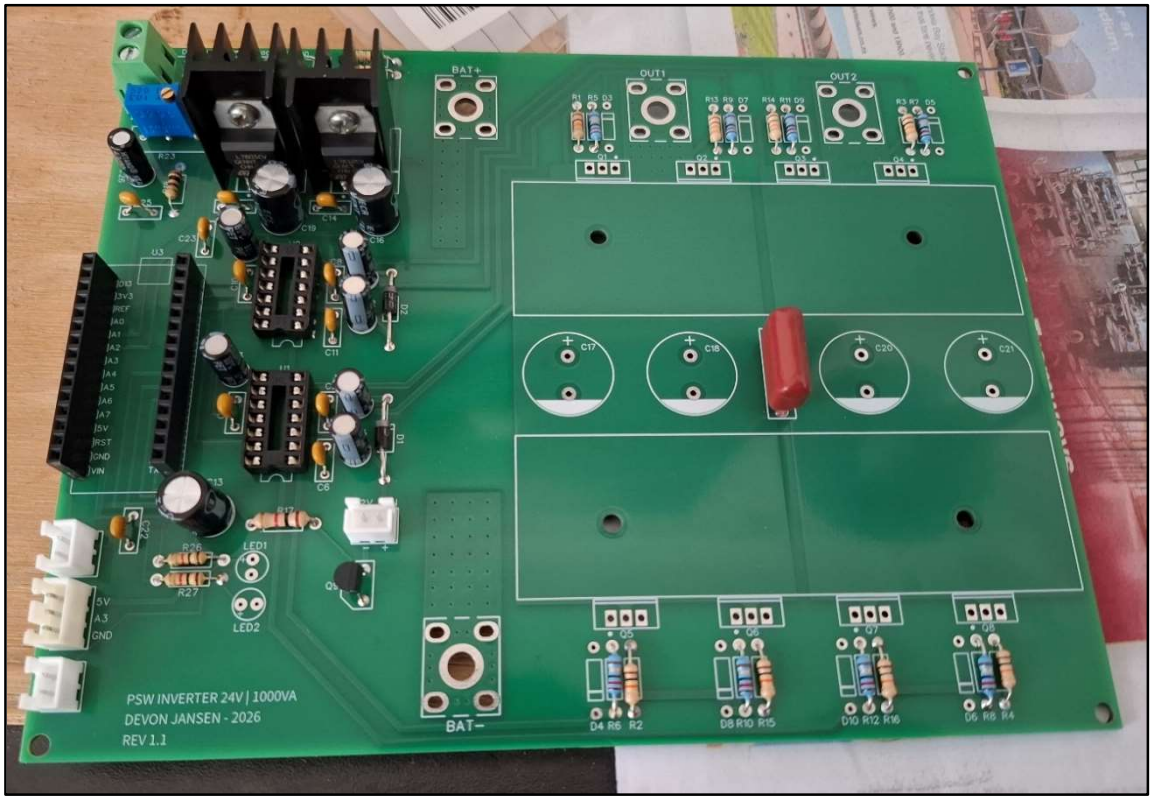


Figure 22: Soldering components



Figure 23: Finished PCB

4.2. Toroidal Transformer Design

This section explains the process of repurposing a faulty 1kVA variac auto-transformer into an isolation transformer (toroidal) suitable for the inverter. The main objective is to have a toroidal transformer that is efficient, quiet and wont saturate under the specified operating conditions. If I design for enough turns to keep the flux density low, the magnetizing current should remain relatively low when driven by a 50Hz sine wave [12]. This results in lower operating temperature, less inrush current on startup, and more importantly reduced core losses because lower flux density cuts down on hysteresis and eddy current losses [12]. While designing for a lower flux density has many advantages, it also requires a core with more cross-sectional area and a higher number of turns.

Transformer parameters	Value
Power rating	1000VA
Primary voltage	14V
Secondary voltage	230V
Frequency	50Hz
Outer diameter (OD)	135mm
Inner diameter (ID)	60mm
Height (h)	55mm

Table 5: Transformer design parameters

In order to achieve these objectives some calculations were needed. First, we need to calculate the cross-sectional area of the toroidal core:

$$A_c = \left(\frac{OD - \mathrm{ID}}{2}\right) * h$$

$$A_c = \left(\frac{135 - 60}{2}\right) * 55$$

$$A_c = 20.6cm^2$$

To limit the risk of core saturation during normal operation a good maximum flux density (Bmax) design target is somewhere between 1T to 1.4T. The selected Bmax value for my transformer was 1.2T. As spoken about previously this results in a sufficiently low idle power consumption and less core losses as opposed to transformers with a higher Bmax. Now that we know the cross-sectional core area, maximum flux density and desired voltage we can calculate the number of turns required for the secondary winding using Faraday's law of induction:

$$N = \frac{V_{\text{rms}}}{4.44 f A_c B_{\text{max}}}$$

$$N = \frac{230}{(4.44)(50)(20.6)(1.2)}$$

$$N = 420\ turns\ for\ the\ secondary\ winding$$

Similarly, we can calculate the number of turns for the primary winding:

$$N = \frac{14}{(4.44)(50)(20.6)(1.2)}$$

$$N = 26\ turns\ for\ the\ primary\ winding$$

The actual maximum flux density after rounding up to 26 turns can be seen below:

$$B_{\text{max}} = \frac{V_{\text{rms}}}{4.44 f N A_e}$$

$$B_{\text{max}} = \frac{14}{4.44(50)(26)(20.6 \times 10^{-4})}$$

$$B_{\text{max}} = 1.177T$$



Figure 25: Insulation between primary and secondary winding

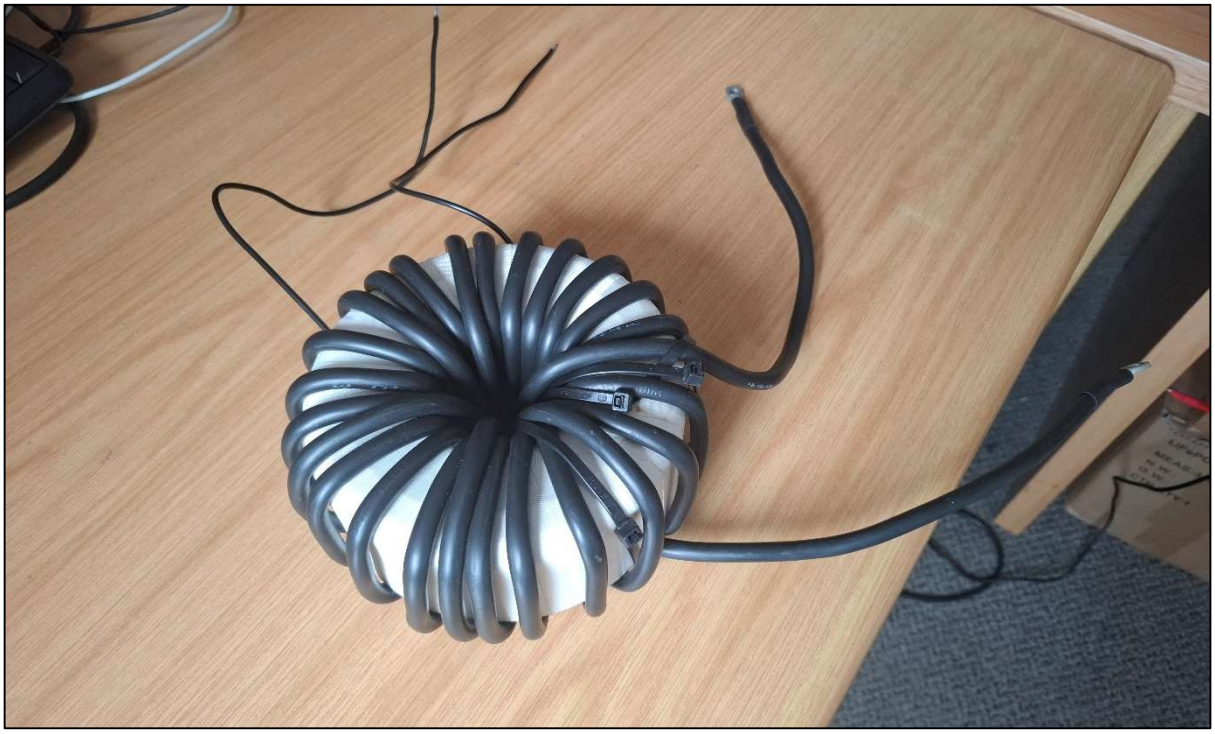


Figure 24: Finished transformer with 26 turns of single flex cable on the primary

4.3. LC Filter design

For transformer-less inverters, LC filter design is relatively straight forward. One would just choose a filter capacitance and calculate for a filter inductance which results in a desired cutoff frequency below the switching frequency and above the fundamental frequency. However, for transformer-based inverters the process becomes much more complex.

A transformer is supposed to be a purely inductive device but practically, that is not the case. Many turns of wire within the same winding sit right next to each other and because a layer of insulation separates them, an electrostatic field forms between the wires resulting in parasitic or stray capacitances [26]. Additionally, transformers will have some leakage inductance which also has to be considered when designing the LC filter.

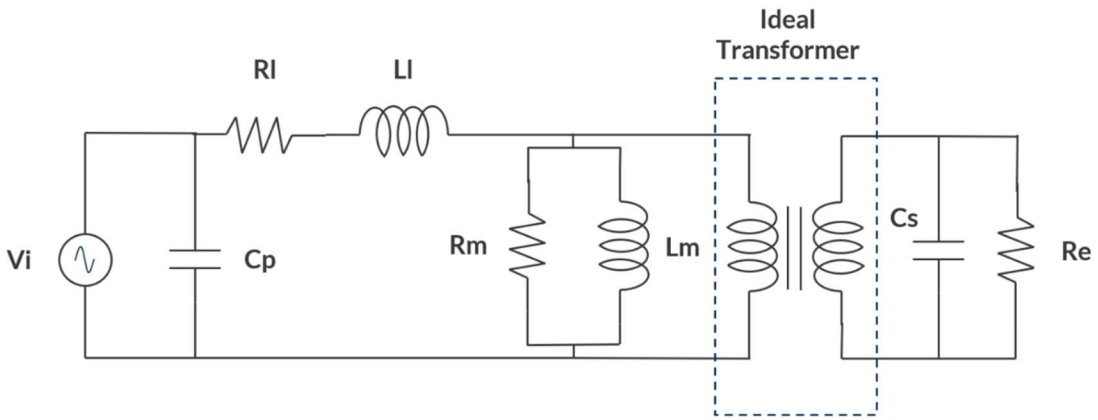


Figure 26: Equivalent circuit of a practical transformer [26]

So, what happens when the transformer primary is connected directly to the low-impedance H-bridge switching at 20kHz? The secondary of the transformer has parasitic capacitance which when reflected back into the primary at the turn's ratio squared, becomes quite significant. This capacitance needs to be charged and discharged 20000 times a second (20kHz) and therefore causes high current spikes every switching cycle. This increases idling current and stresses the MOSFETs unnecessarily.

This is why I fit the series filter inductor on the primary side to oppose the sudden changes in current and block most of the high-frequency PWM from being fed directly into the transformer. With sufficient series inductance, the high frequency PWM can be quite well isolated from the low frequency transformer primary. Now on one side of the choke, you can see the high frequency PWM and on the other side you can see a 50Hz sine wave with some small amounts of high frequency ripple shown in the oscilloscope screenshots taken below.

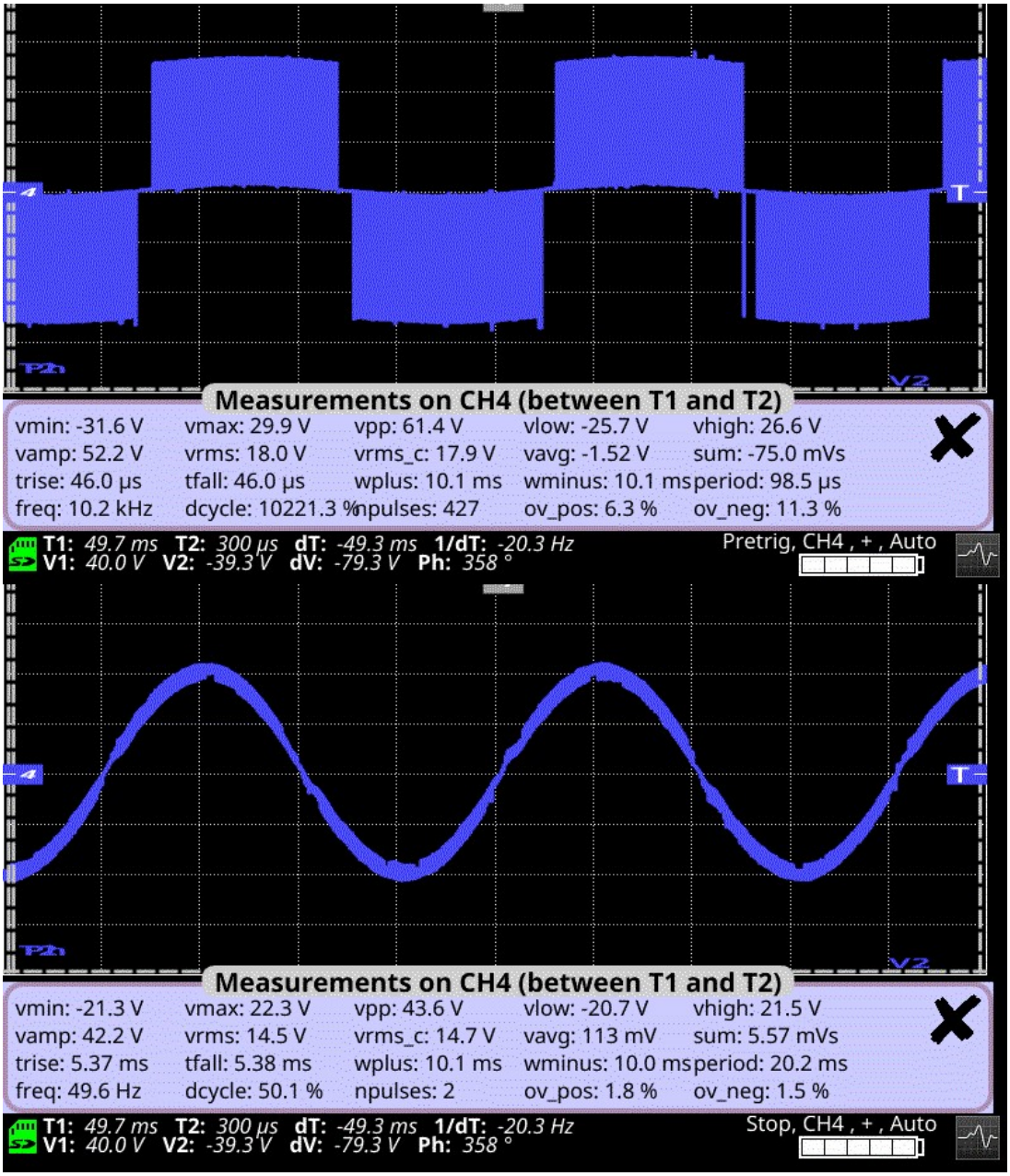


Figure 27: Before and after the choke (68uH used)

Now you might assume that the shunt filter capacitor is going to be directly after the filter inductor on the transformer primary. However, this can't be done because an incredibly large capacitor would be needed which is impractical and not feasible. Using transformer equivalent circuit theory, the capacitance on the secondary is reflected over to the primary using the turns ratio squared [11]. Using a filter capacitance of 2.2uF on the secondary, the reflected capacitance on the primary can then be calculated as:

$$C_p = \left(\frac{V_s}{V_p}\right)^2 C_s$$

$$C_p = \left(\frac{230}{14}\right)^2 \times (2.2 \times 10^{-6})$$

$$C_p = 593.88uF$$

Therefore, the use of a series inductor on the transformer primary and a parallel capacitor on the transformer secondary allows for a much smaller filter capacitor value. Next, a sufficient cutoff frequency should be chosen for the filter which is above the fundamental 50Hz and well below the 20kHz switching frequency. A cutoff frequency of 900Hz was chosen and used together with the reflected capacitance to calculate filter inductance.

$$f_c = \frac{1}{2\pi\sqrt{L_p C_p}}$$

$$L_p = \frac{1}{(2\pi f_c)^2 C_p}$$

$$L_p = \frac{1}{(2\pi \times 900)^2 (593.88 \times 10^{-6})}$$

$$L_p = 52.66uH$$

Two **Sendust** also known as **Kool Mu** toroidal cores were stacked on top of each other to increase the total core cross-sectional area. This has a number of benefits including the reduction of turns needed and more headroom before saturation. At max load the choke can have up to 70A of current flowing through it, and I don't want it to saturate too quickly. The choke was wound and measured as 56.25uH which is slightly higher than our calculations but is still sufficient.



Figure 28: Measuring series inductance of wound choke

4.4. Cooling and Protection

Under load the temperature of the MOSFETs, choke and transformer increase with time, and with a rise in temperature there is an increase in resistance. Higher resistance results in more power losses and lower efficiency. To combat this, large heatsinks were installed and a temperature-controlled fan was implemented. As can be seen in the figure below, an NTC thermistor was attached to the heatsink and if the measured temperature increases above 30 degrees the 12V fan is turned on. A 63A DC circuit breaker was also installed between the battery bank and the inverter for protection against overload and short-circuits.

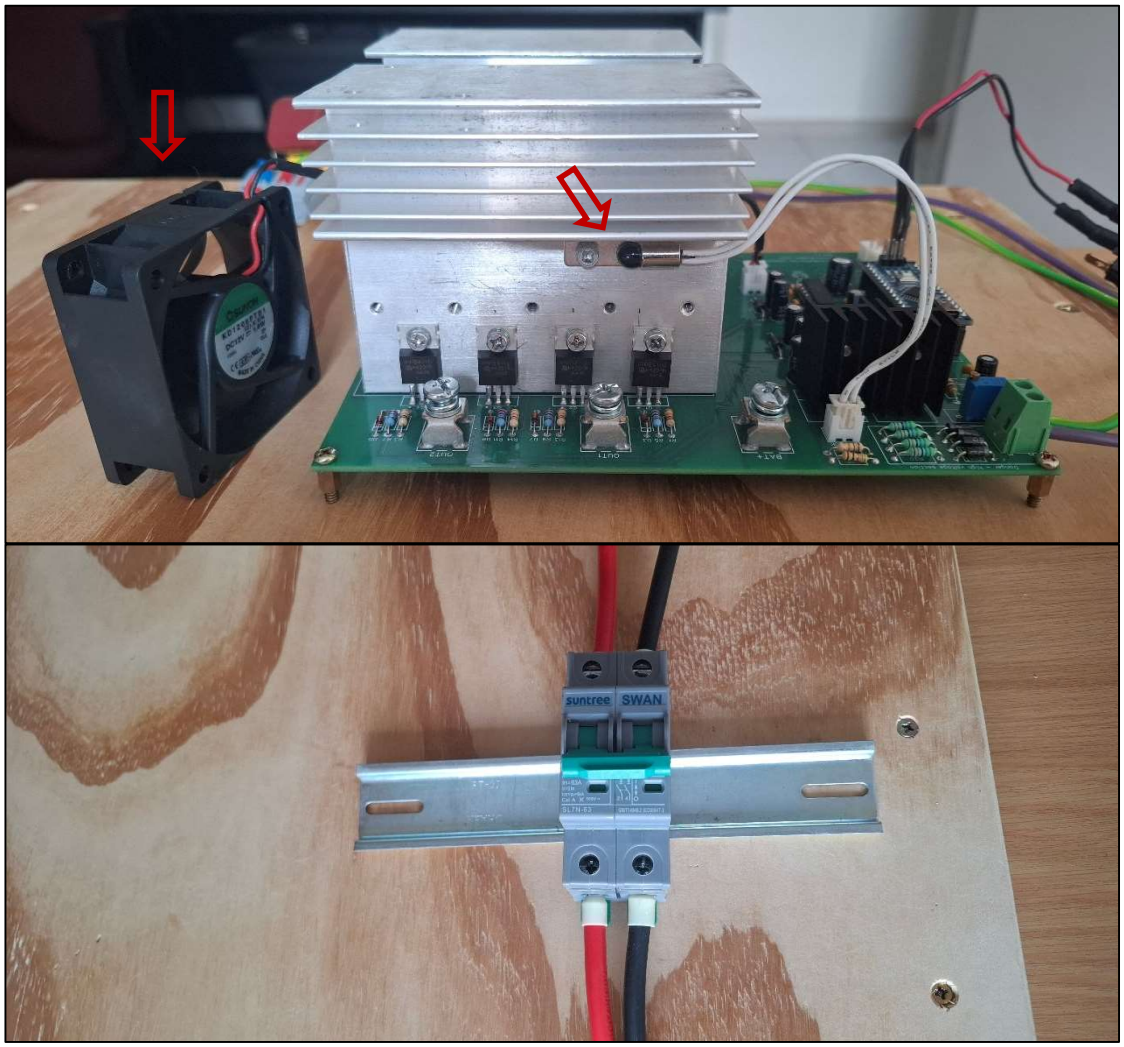


Figure 29: Cooling and protection

5. Control and software implementation

5.1. Implementation of PID Controller

The PID controller uses a feedback circuit which takes the AC output voltage, rectifies it, sends it through a voltage divider and low pass filters it. This DC feedback signal represents the measured output voltage where 3V DC at the ADC of the microcontroller is the equivalent to 230V AC at the inverter output. This allows the controller to compare the measured voltage against a constant reference rather than a sinusoidal one. The control loop operates at a sampling frequency of 100 Hz (T_s = 0.01s).

The error is calculated using:

$$e[k] = setpoint - measured\ voltage[\text{k}] \tag{7}$$

The proportional term is calculated using:

$$P[k] = K_p e[k] \tag{8}$$

The trapezoidal integration method was selected to calculate the integral term in discrete time. Unlike a simple rectangular integration method, it considers both the present and previous error values.

$$I[k] = I[k-1] + \frac{K_i T_s}{2}(e[k] + e[k-1]) \tag{9}$$

To prevent excessive integral accumulation, anti-windup was implemented where additional integral terms were limited if the maximum or minimum modulation index was reached.

The derivative term is calculated from the change in measured voltage rather than the error directly and also uses a digital filter to reduce the effects of noise.

$$D[k] = \frac{-2K_d(y[k] - y[k-1]) + (2\tau - T_s)D[k-1]}{2\tau + T_s} \quad (10)$$

Where τ represents the derivative filter time constant. The controller output is then calculated and added to the modulation index:

$$output[k] = P[k] + I[k] + D[k] \quad (11)$$

The modulation index is then limited between 0.01 and 0.98 to prevent over and under modulation.

```
// Calculate error
error = setpoint - voltageFeedback;

// Proportional term
P = Kp * error;

// Integral term
float newI = I + Ki * (T / 2.0f) * (error + prevError);

// Derivative term (filtered)
D = (-2.0f * Kd * (voltageFeedback - prevVoltageFeedback) + (2.0f * tau - T) * D) / (2.0f * tau + T);

// Controller output
output = P + I + D;

// Integral anti-windup
if (percentMod >= maxMod) {
  if (error < 0.0f) {I = newI;}
}
else if (percentMod <= minMod) {
  if (error > 0.0f) {I = newI;}
}
else {
  I = newI;  // Not saturated, integrate normally
}

// Update modulation index
percentMod += output;
```

Figure 30: PID controller in code

5.2. Implementation of PR Controller

Unlike the PID implementation, which used a rectified and filtered DC feedback signal, the PR controller used instantaneous AC voltage measurements obtained through a ZMPT101B voltage sensor module. The module uses a small 1000:1000 turns ratio transformer and an op-amp for biasing with a +2.5V DC offset [27]. The measured output voltage is continuously compared against a sinusoidal reference signal operating at the fundamental output frequency of 50 Hz. The calculated error is then used to generate a correction to the inverter modulation index.

For the inverter prototype, a non-ideal PR controller was selected. This configuration makes use of a small resonant bandwidth chosen to be $\omega_c = 3rad/s$ or approximately 0.5Hz. This allows the controller to maintain high gain around 49.5-50.5 Hz while avoiding the theoretically infinite gain associated with an ideal resonant controller. The selected sampling frequency was 250 Hz (T_s = 0.004s). Higher sampling times were tested but the controller became unstable.

The sinusoidal reference generated in code can be represented by:

$$v_{\text{ref}}(t) = V_{\text{peak}} \sin(\omega_0 t) \tag{12}$$

Where the peak reference voltage is $(230)(\sqrt{2}) = 325.27$ V and the fundamental angular frequency is $(2\pi)(50) = 314.16$ rad/s. The controller error and proportional term is calculated the same way as the PID controller which can be seen in equation 7 and 8. The resonant term is implemented using the following transfer function:

$$\text{R} = \frac{2K_r\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \tag{13}$$

Before running the inverter with the PR controller active, I had to ensure that the feedback signal and sinusoidal reference were in phase. Any phase difference

introduces an additional tracking error, even when the output voltage is relatively close to the desired reference [28]. The serial plotter within the Arduino IDE was used to see both the feedback signal (orange) and the sinusoidal reference (blue). In figure 31, we can see that they are out of phase by about 28.6 degrees. This was addressed by synchronising the sinusoidal reference generation with the PWM generation. Correct phase alignment is very important for PR control because its resonant term is designed to provide high gain at the fundamental reference frequency but if the inverter frequency is slightly out, a huge drop off in resonant gain will occur [28]. After this was completed the PR controller was manually tuned to find controller gains (Kp and Kr) which resulted in stable voltage regulation without excessive oscillations.

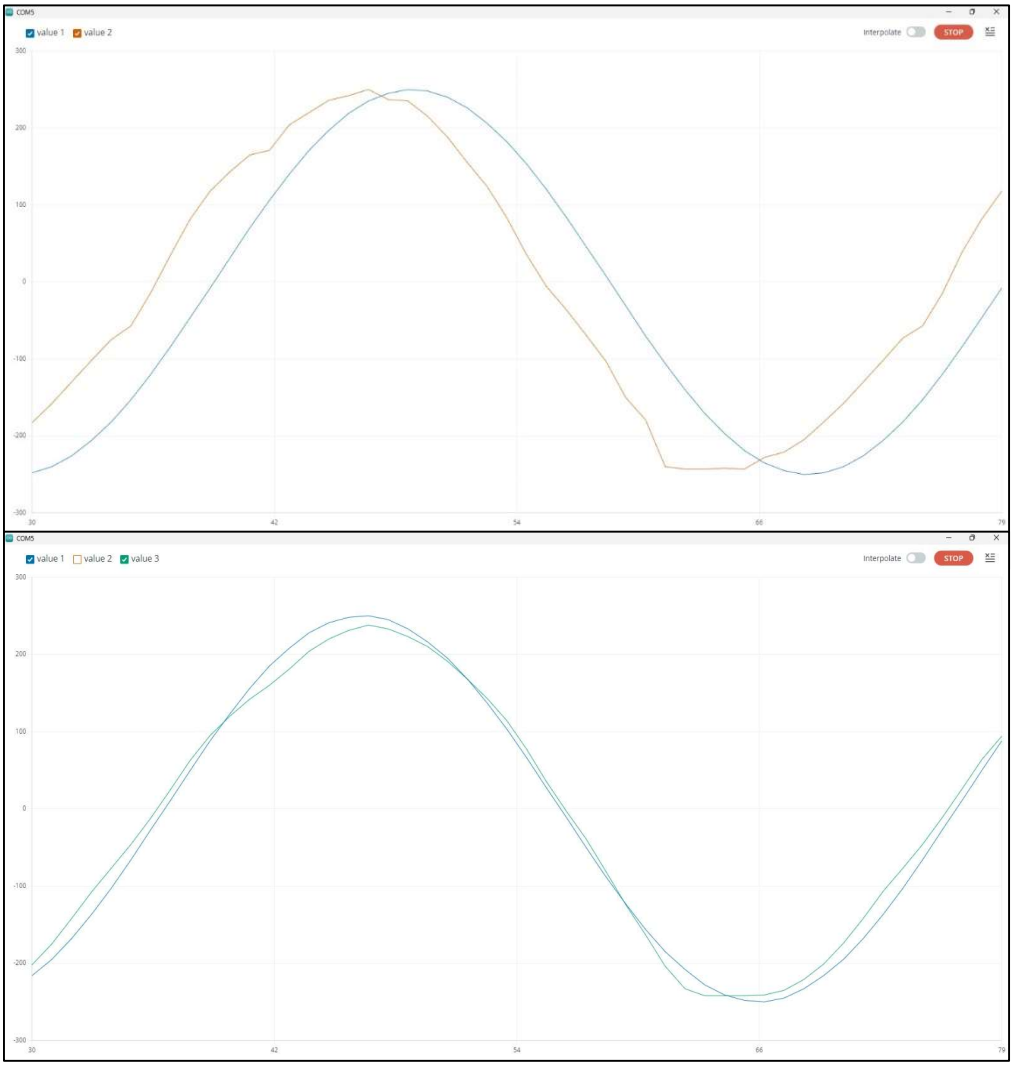


Figure 31: Feedback signal and reference before and after phase matching

6. Results and Analysis

6.1. Experimental setup

In order to get experimental testing underway, the prototype was setup with all the necessary measurement equipment. My laptop was connected to the inverter's microcontroller (Arduino Nano) in order to record timed data points and display feedback measurements on the Arduino IDE serial monitor. After each test, these timestamped data points were uploaded to MATLAB, and a script was run which would plot graphs and write the data to excel spreadsheets.

In the figure below you can see two 12V 100Ah batteries connected in series for a 24V DC supply. The battery bank is connected to the H-bridge and control board (green PCB) separated by a 63A DC circuit breaker. The rest of the setup and measurement tools can be seen on the following page.

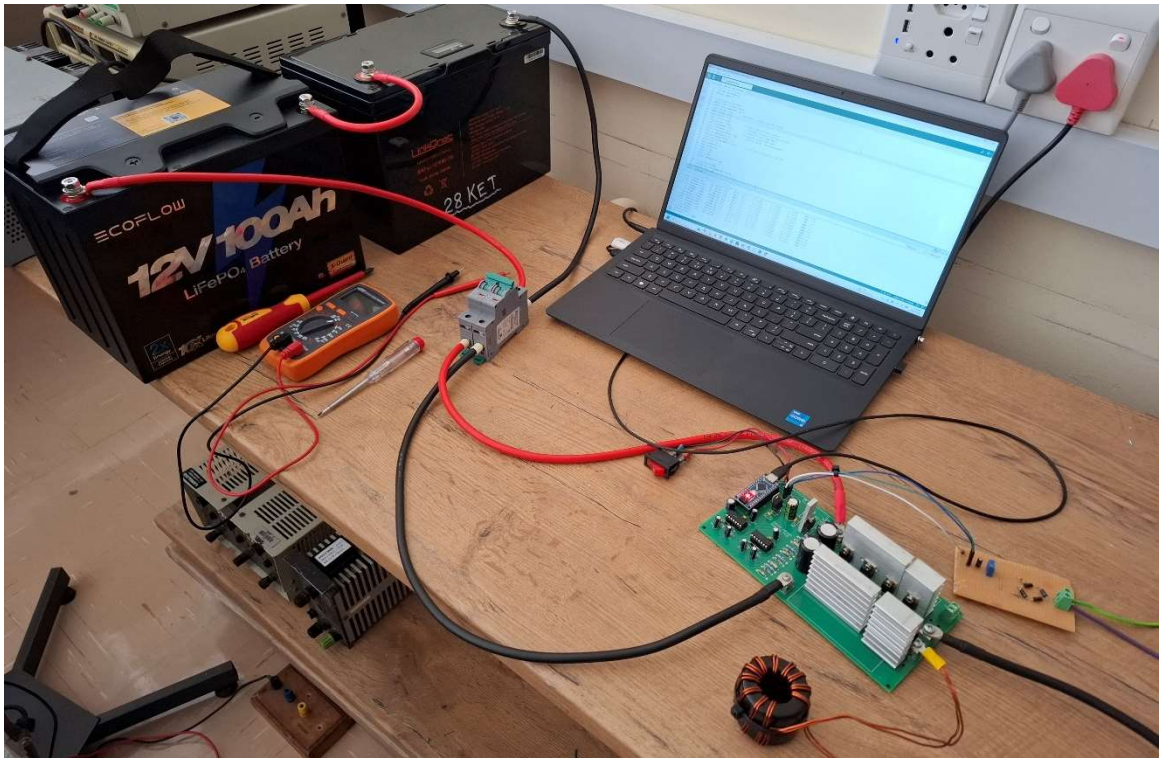


Figure 32: Experimental setup left side

The H-bridge output is connected to the transformer primary with the series filter inductor (56.25uH) inbetween. On the secondary of the transformer, two filter capacitors (1uF and 2.2uF for a total of 3.2uF) are used, aswell as the load box consisting of incandescent light bulbs. An oscillscope was used to read the output voltage, freqeuncy and THD and micro-SD card was used to retrieve oscilloscope screenshots for documentation. A multimeter was used to read the DC input voltage and a current clamp-meter was used to measure both the input DC and output AC currents.

Measurement instruments used:

- Oscilloscope: Scopix IV 0x9104
- MTD10 multimeter
- Kaiweets HT206 current clamp-meter
- LCR meter

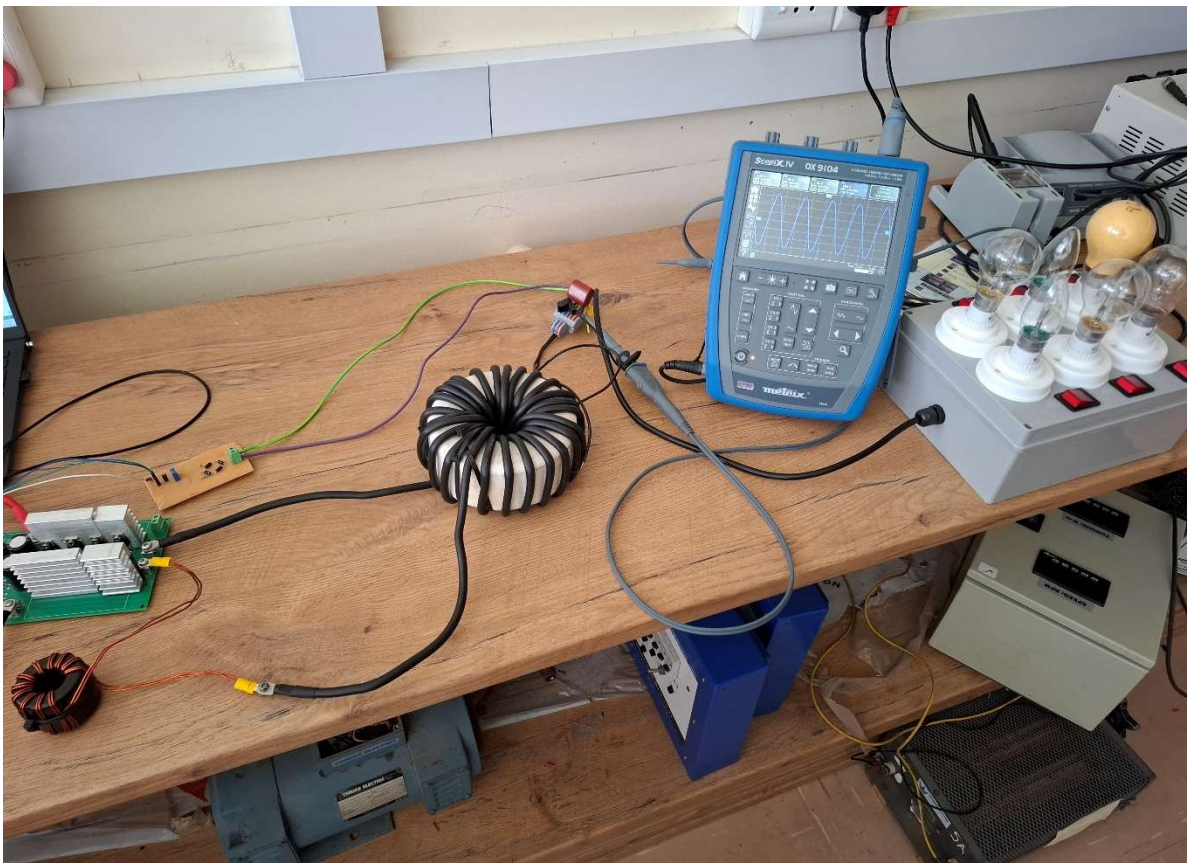


Figure 33: Experimental setup right side

6.2. Open Loop Results

Figure 34 below, shows the measured open-loop RMS output voltage during the inverter start-up where a 70W resistive load disturbance was put on at around 4.6s and another 70W load at 7s. The inverter initially uses a software implemented soft start which progressively increases the modulation index until it reaches approximately 230V RMS over the course of 2.5s. The purpose of the soft start is to minimize the transformer's magnetizing inrush current which often causes an initial voltage spike that can damage MOSFETs and other components.

Once the soft start is complete, the output remains at approximately 230V RMS until the first 70W load is turned on at 4.6s. The output voltage drops and settles at 219V, well below the 230V setpoint. Later on, at 7s another 70W load is added for a total of 140W, and the voltage drops to 216V. The important finding was that the output voltage will continue to drop as the load increases and will not automatically return to its reference or setpoint value.

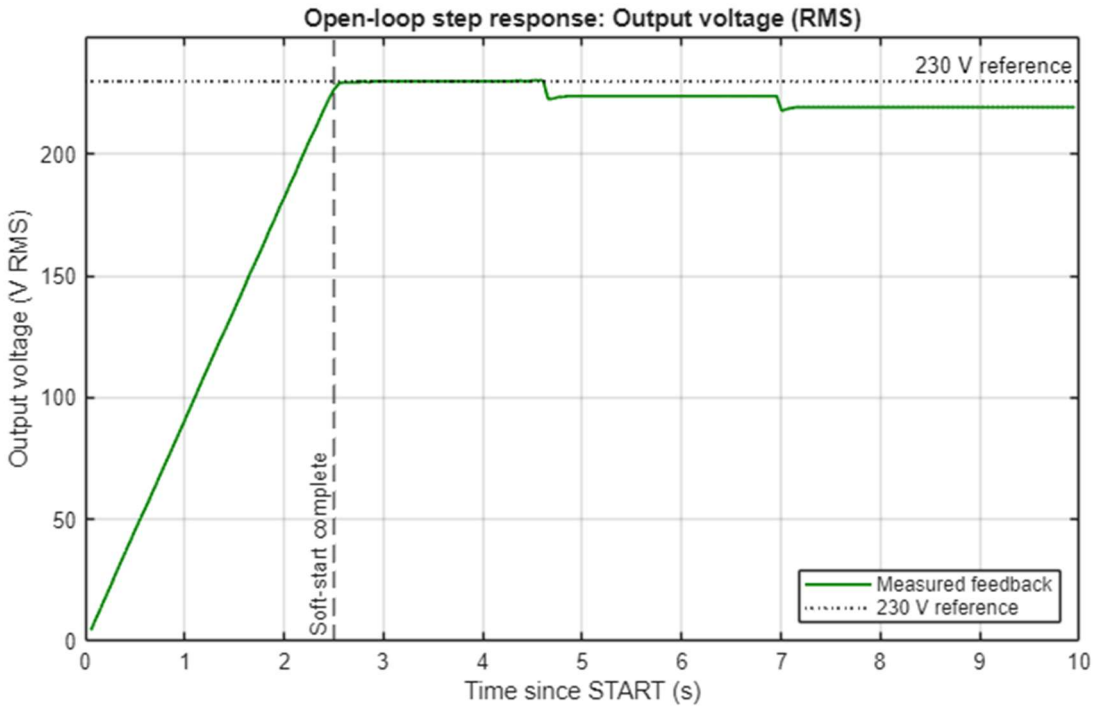


Figure 34: Open-loop step response with load disturbances at 4.6s and 7s

The reduction in output voltage is caused by many factors including internal impedance of the DC supply, MOSFET conduction losses and transformer winding resistance to name a few. As the load is increased, current draw is increased and any resistance in the circuit will cause a voltage sag in the DC supply. This can be somewhat negated by using a very large and stiff DC supply with minimal internal resistance, but the issue will still persist to some degree. Since the inverter is operating without closed loop control, nothing is being done to compensate for these losses. These results highlight a major limitation of open-loop inverter operation and show us the importance of implementing a well-designed closed-loop controller.

Test	Load (W)	Setpoint Voltage	Voltage After Load	Voltage Drop (%)
1	70	230	219	4.78
2	140	230	216	6.09
3	200	230	212	7.83
4	240	230	208	9.57
5	300	230	206	10.43

Table 6: Open-loop results

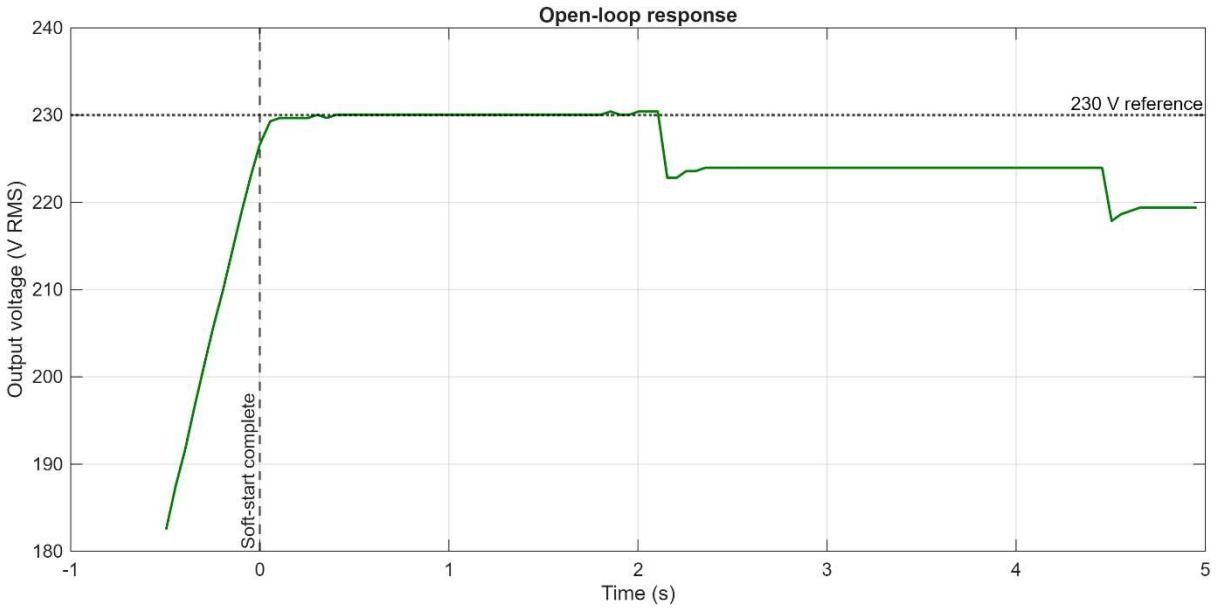


Figure 35: Open-loop transient response

6.3. PID Control Results

Figure 36 below shows the inverter's output voltage step response after closed-loop PID control was implemented and controller gains were manually tuned. Once the soft start procedure is complete and the PID controller is enabled at 2.5s, a small transient disturbance can be seen with some overshoot. This happens at the transition between the soft start and PID being enabled where a small error needs to be corrected by the controller.

After about 2.6s, the measured voltage remains close to 230V RMS, showing a near zero steady-state error. A 70W load was introduced at around 6.7s resulting in a small voltage dip and then slight overshoot after PID performs the correction. Despite the load disturbance, the controller returns the output back towards the 230V AC setpoint without excessive oscillation which is a major improvement over the open-loop operation tests. On the next page a more zoomed in screenshot can be seen of the same test with smaller voltage divisions and timescale.

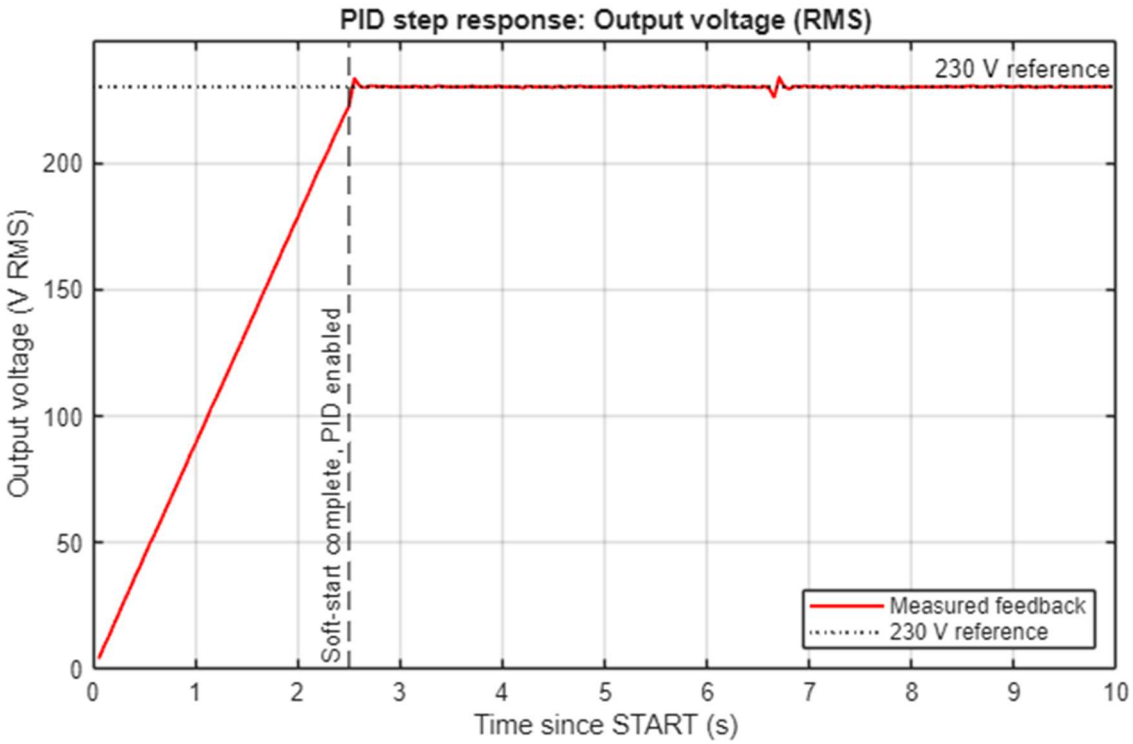


Figure 36: Manually tuned PID controller step response (test 3)

Figure 37 below provides a closer look at the PID controller response seen on the previous page. In test 3, the maximum recorded voltage was 233.24V corresponding to an overshoot of 1.409% when compared to the 230V reference. The minimum voltage recorded was found to be 225.9V after the load disturbance was introduced which is a reduction of 1.78% below reference and the steady state voltage came out as 229.62V which is a 0.165% steady-state error. All of these results were computed by a MATLAB script using data points uploaded from my microcontroller, so there is no chance of human error when calculating for overshoot, steady-state error, settling time etc.

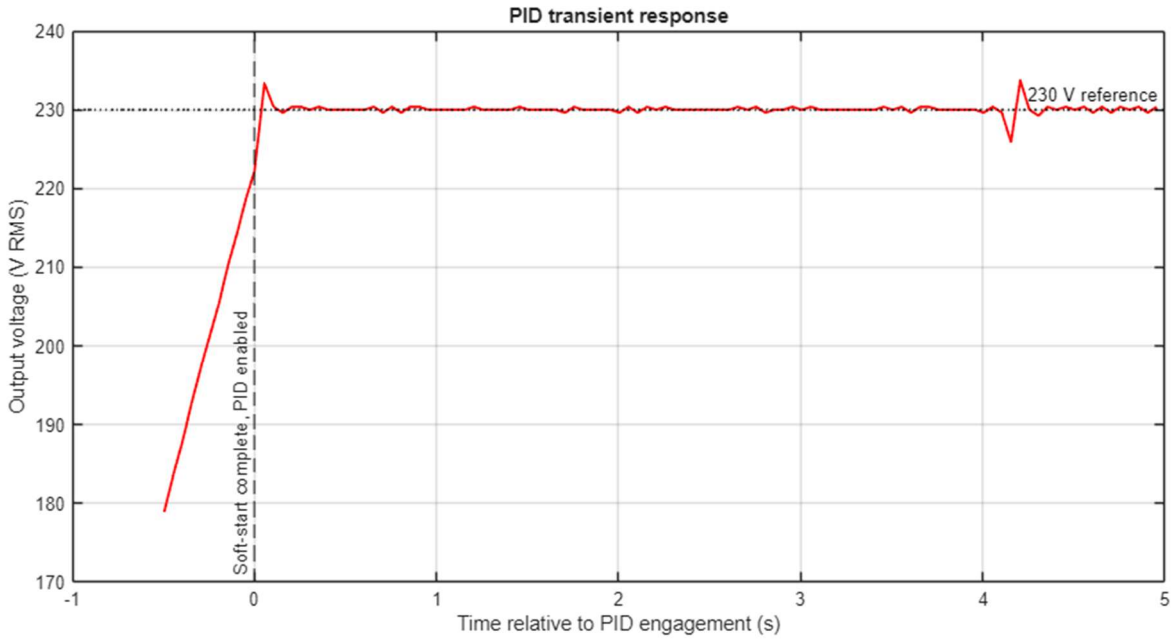


Figure 37: PID transient response (Test 3)

In figure 38 and 39 the contributions of each controller term P, I and D are plotted. In test 3, Kd was set to 0 (PI control) and in test 8, Kd was set to 0.05. Note, how the derivative term makes up most of the control effort in test 8. It was also found that a small Kd gain (less than 0.02) acted as a dampener, reducing overshoot and resisting sudden changes in the controller output, but when Kd was set too high oscillations occurred.

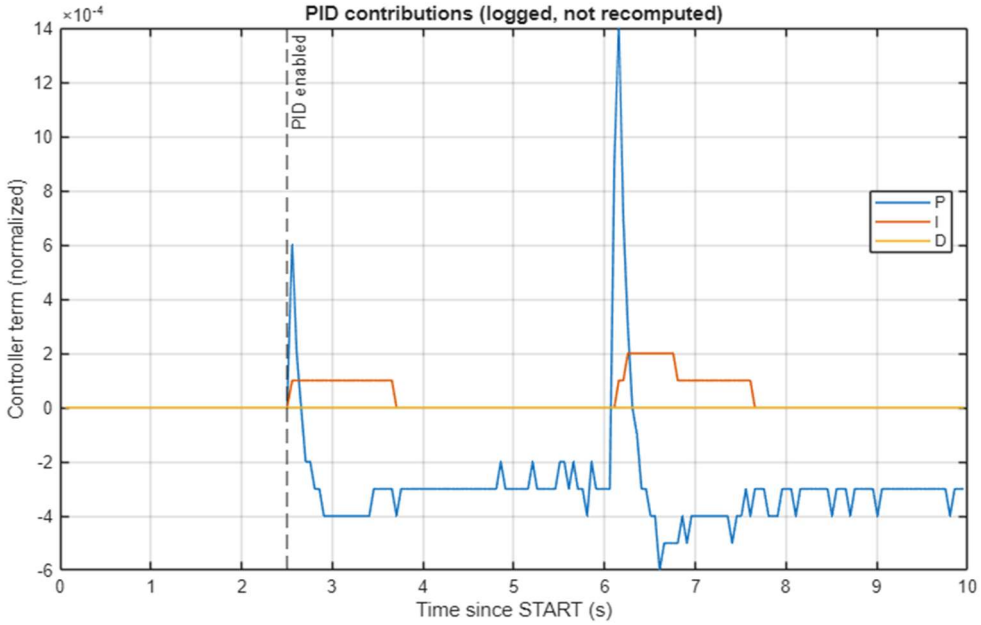


Figure 38: Test 3 PI contributions

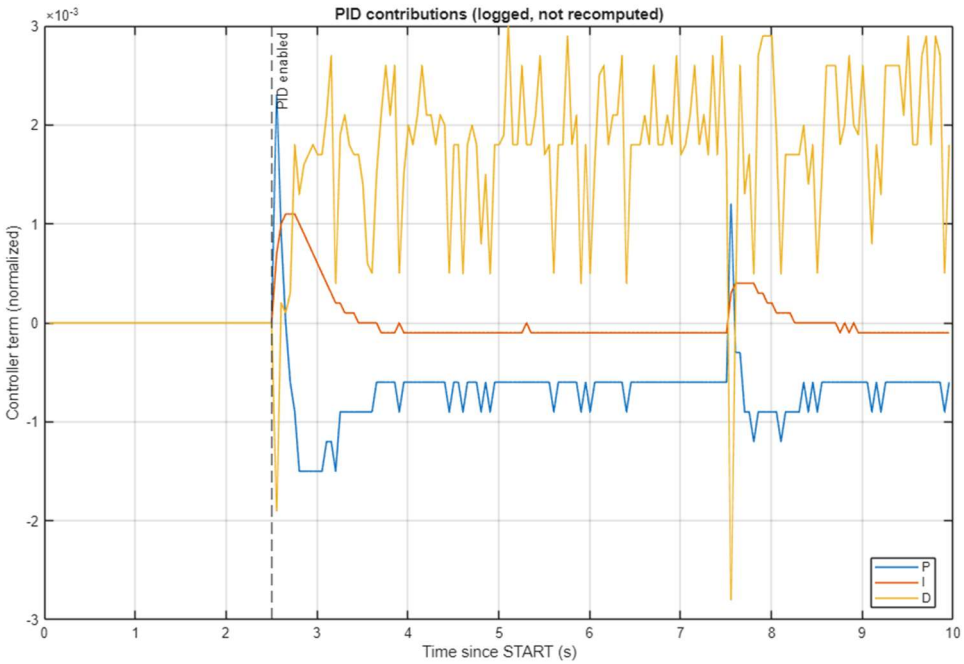


Figure 39: Test 8 PID contributions

Test	Kp	Ki	Kd	Load (W)	Setpoint Voltage	Steady-State Voltage	Steady-State Error (%)	Settling Time - 2% (s)	Peak Voltage	Overshoot (%)	Minimum Voltage
1	0.1	0.1	0	70	230	230.2	0.087	2.9	231.12	0.487	224.4
2	0.3	0.15	0	70	230	230.37	0.161	2.7	231.12	0.487	224.78
3	0.6	0.2	0	70	230	229.62	-0.165	2.6	233.24	1.409	225.9
4	0.9	0.3	0	70	230	230.1	0.043	2.7	232.61	1.135	225.154
5	1	0.5	0	70	230	229.254	-0.324	2.8	233.35	1.457	228.509
6	0.1	0.6	0.01	70	230	229.62	-0.165	3.5	232.24	0.974	223.29
7	0.3	0.8	0.02	70	230	230.37	0.161	3.6	231.12	0.487	226.64
8	0.6	1	0.05	70	230	Nan	Nan	Nan	235.2	1.826	222.4
9	0.9	2	0	70	230	230.2	0.087	2.6	232.98	1.296	227.391
10	1	3	0	70	230	230.4	0.174	2.6	233.73	1.622	226.28

Table 7: PID control results

The PID controller was initially tested using ten different combinations of controller gains, with each test introducing a 70W resistive load disturbance sometime during the operation of the inverter. For nine of the ten configurations, the steady-state error remained below 0.33% with test 4 reaching as low as 0.043%. This is a significant improvement over the open-loop results where the output voltage dropped to 219V after the 70W load was introduced and remained there.

In Test 1, I started off small with a Kp and Ki of 0.1 which produced a steady-state voltage of 230.2 V, an overshoot of 0.487% and a settling time of 2.9 s. When the proportional and integral gains were increased in later tests, the controller still maintained a near zero steady-state error but an increase in overshoot could be seen. For example, test 5 used a Kp and Ki of 1 and 0.5 respectively where the resulting overshoot increased to 1.457%, compared with 0.487% in test 1. This shows the trade-off that comes with increasing controller responsiveness. Although larger controller gains can improve the correction of voltage deviations quicker, it can also cause increased overshoot and instability.

Test 8 resulted in an unstable system which oscillated between 222.4V and 235.2V, never quite reaching steady state. This occurred when Kd was increased to 0.05 and higher Kd values were not tested for the safety of my hardware. The results showed that a PI controller often performed better than a PID controller, and if a derivative gain is to be introduced for its dampening effects it should be very small.

Tests 9 and 10 produced the shortest settling times of 2.6 seconds. Both configurations maintained small steady-state errors, but test 10 resulted in a higher overshoot of 1.622%, compared with 1.296% for test 9. Test 9 is particularly noteworthy because it achieved a steady-state voltage of 230.2 V RMS, an absolute steady-state error of only 0.087%, a settling time of 2.6 seconds and a minimum voltage of 227.391 V RMS. Therefore, test 9 represents a promising controller configuration for a good balance in voltage regulation, overshoot, settling time and minimum voltage.

6.4. PR Control Results

Figure 40 plots the measured RMS output voltage when the inverter is operating with the manually tuned proportional-resonant controller. An ideal PR controller is designed to provide infinite gain around a specified resonant frequency, which in this case is the 50 Hz fundamental output frequency. This can lead to instability in practical applications and therefore a damping term also known as a resonant bandwidth was introduced where $\omega_c = 3$ rad/s.

Similarly to the PID controller the initial changeover from the soft start procedure to PR control results in a slight overshoot as the controller stabilizes. At 5.7s a 70W load disturbance was introduced where the voltage dips sharply before recovering back towards the setpoint. Although the controller recovers well, the transient was definitely more pronounced than the PID test 3 step response plot.

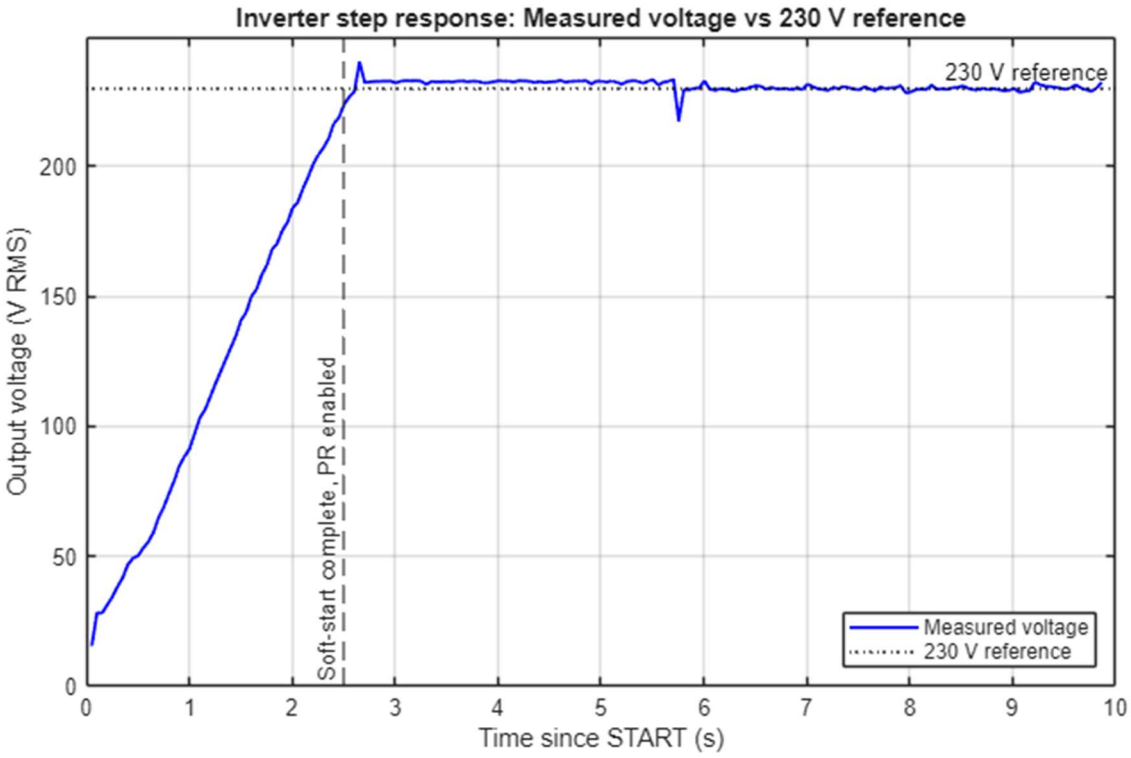


Figure 40: Manually tuned PR controller step response (test 3)

Figure 35 shows a better view of the PR controller's transient behaviour, allowing the overshoot, voltage fluctuations and disturbance response to be seen in more detail. After tabulating the MATLAB script results, we can see that test 3 for the PR controller has the maximum voltage coming out as 240.21V which is a 4.44% overshoot. The absolute minimum voltage dip caused by load application came out as 218.73V. These results indicate that the chosen PR gains (Kp=0.6, Kr=0.2) during this test provide less effective disturbance rejection than the equivalent PI gains (Kp=0.6, Ki=0.2). However, we cannot fairly compare two controllers using the same gains no matter how similar they are. Therefore, more testing was done, and results were tabulated as can be seen later in this section.

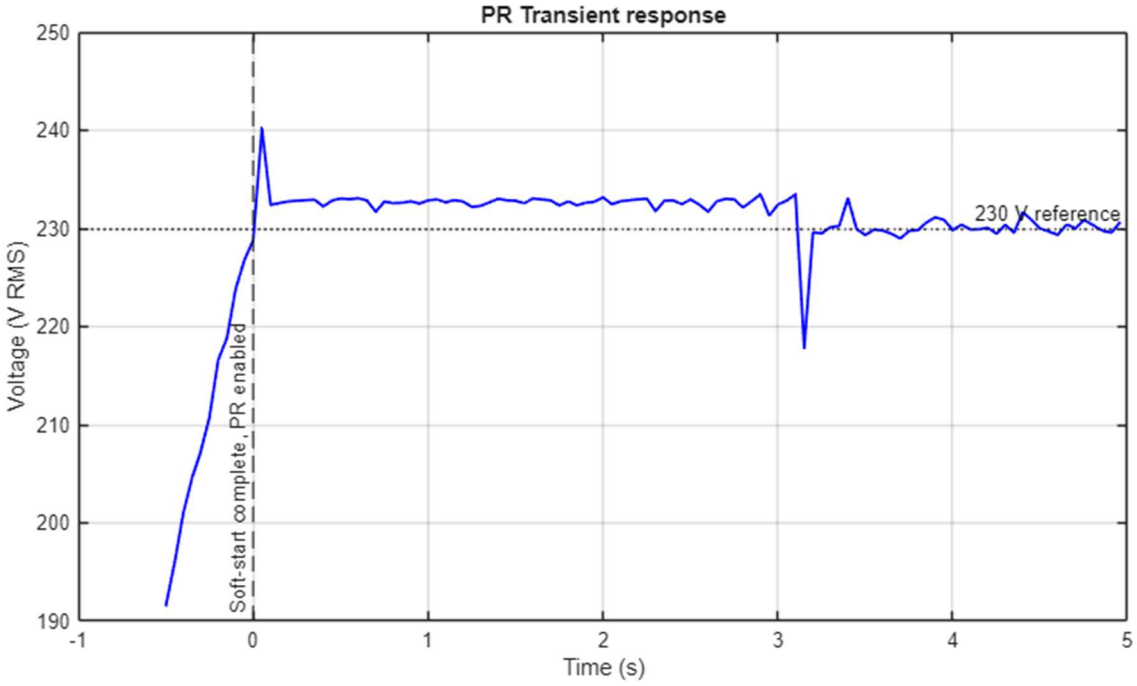


Figure 41: PR transient response (test 3)

In order to truly see how the PR controller performed we would need to introduce a larger load disturbance. Figure 36 is the PR controller step response when subjected to a 300W resistive load after being manually tuned. Before the disturbance, the measured output voltage remains fairly close to the 230V reference with a small steady state error of 0.152%. Once the load is turned on at 5.8s, the voltage momentarily drops down to 205.4V and then recovers back to the setpoint with minimal overshoot. This was a very promising result for the PR controller, but further tuning would be necessary in order to improve disturbance rejection because even a momentary voltage dip or overshoot can damage some sensitive appliances.

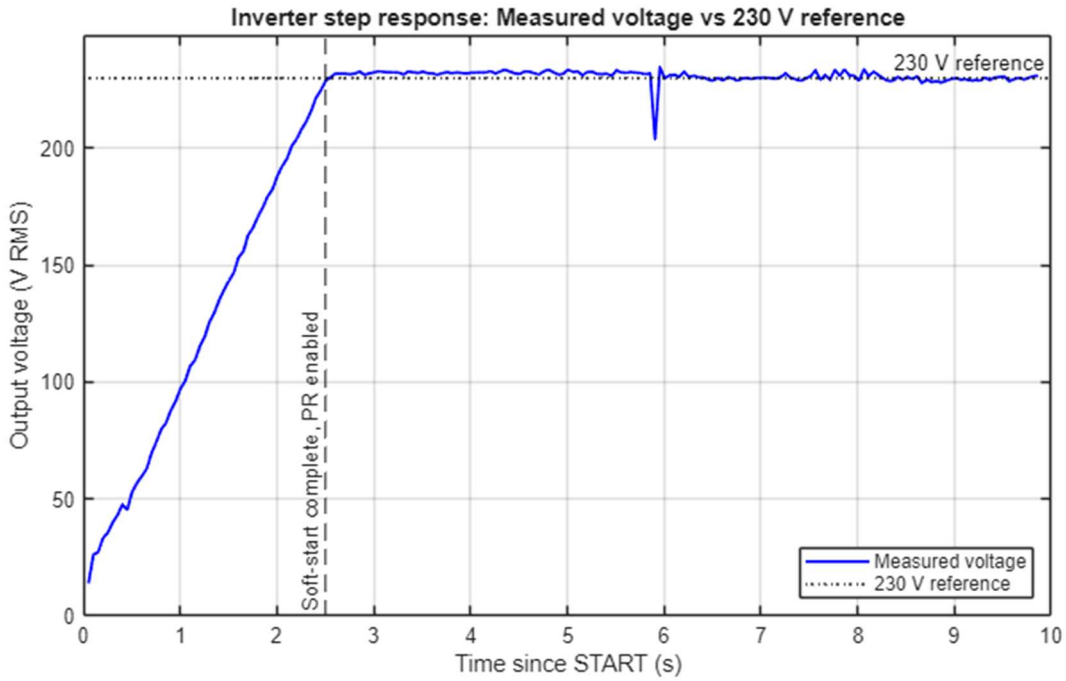


Figure 42: PR step response with 300W load disturbance

Figure 43 shows the PR controller step response for test 10, which used a proportional gain of 1 and a resonant gain of 0.9. Unlike the other test results, the measured output voltage started to oscillate. These oscillations seem to indicate that the chosen controller gains are causing excessive error correction, and the modulation index is being changed too aggressively. Test 10's tabulated results towards the end of the section do not provide a steady state error or settling time because the controller never settled. The controller gains were never increased further than this for the safety of my hardware.

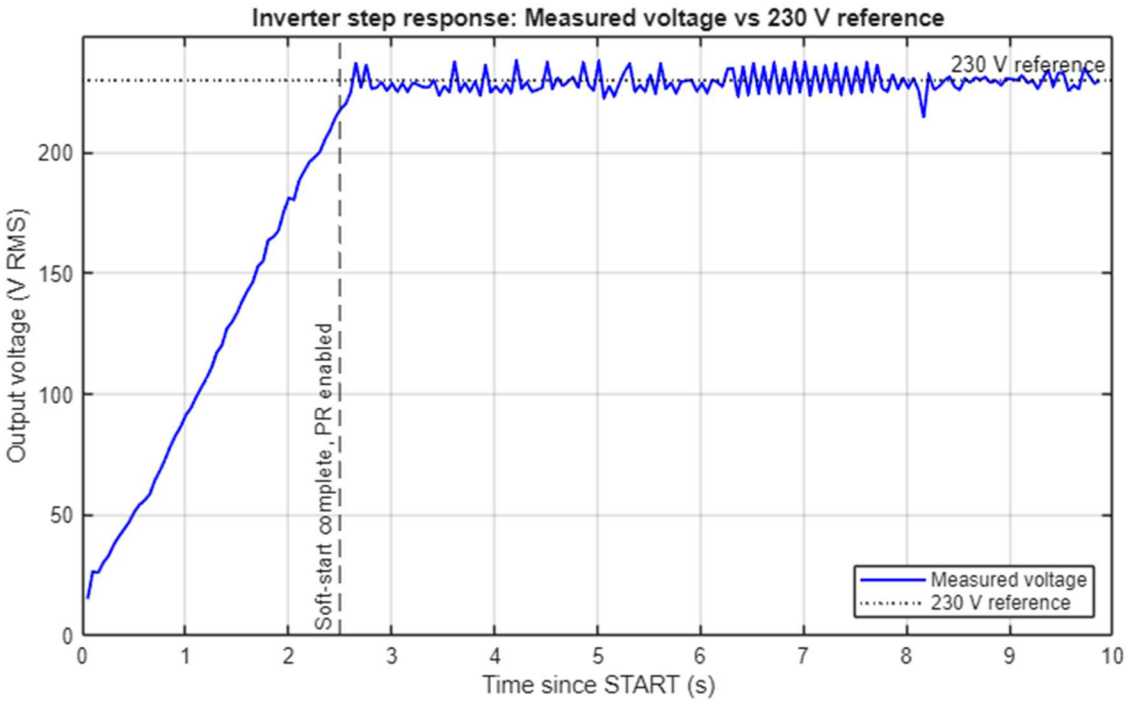


Figure 43: Oscillatory PR controller response (Test 10)

Test	Kp	Kr	Load (W)	Setpoint Voltage	Steady-State Voltage	Steady-State Error (%)	Settling Time - 2% (s)	Peak Voltage	Overshoot (%)	Minimum Voltage
1	0.1	0.1	70	230	230.35	0.152	5.4	235.88	2.56	228.6
2	0.3	0.15	70	230	230.1	0.043	5.2	236.18	2.69	207.4
3	0.6	0.2	70	230	230.16	0.070	2.6	240.21	4.44	218.83
4	0.9	0.3	70	230	230.33	0.143	5.002	240.14	4.41	207.58
5	1	0.4	70	230	229.59	-0.178	7.6	239.86	4.29	207.2
6	0.1	0.5	70	230	230.1	0.043	6.2	234.72	2.05	225.2
7	0.3	0.6	70	230	229.37	-0.274	2.65	234.39	1.91	215.8
8	0.6	0.7	70	230	229.57	-0.187	2.62	234.7	2.04	204.04
9	0.9	0.8	70	230	229.87	-0.057	2.6	236.67	2.90	219.67
10	1	0.9	70	230	Nan	Nan	Nan	238.29	3.60	214.78

Table 8: PR control results

The PR controller was tested with a 70W load disturbance using ten different combinations of proportional and resonant gains and the results were recorded and calculated in MATLAB. For the nine tests with steady-state voltage results, the measured voltage ranged from 229.37 V to 230.35 V RMS. Therefore, the steady-state error remained below 0.28% for all nine of these tests. The results also show that the resonant gain (Kr) has a strong relationship with the transient behaviour of the controller.

Tests 1 and 2 produced relatively small overshoot values of 2.56% and 2.69%, but their settling times were quite long at 5.4 seconds and 5.2 seconds. Test 3 produced a shorter settling time of 2.6 seconds, but its overshoot increased to 4.44%. This means there is a trade-off between the settling-time performance and overshoot for the different configurations tested. Tests 7 and 8 achieved settling times close to 2.6 seconds but lacked performance in other areas. For example, test 8 recorded a minimum voltage of 204.04 V RMS, which is a massive reduction of 11.29% below the reference.

Test 9 produced a steady-state voltage of 229.87 V RMS, an error of 0.057%, a settling time of 2.6 seconds and an overshoot of 2.90%. Test 9 provides a good balance between steady-state accuracy and settling time among the PR configurations. Test 10's selected controller gains were not suitable for stable voltage regulation as the measured voltage oscillated around the setpoint, never reaching steady state.

Overall, the PR results show that good steady-state RMS voltage regulation can be achieved but the controller response is very sensitive to the selected proportional and resonant gains. In theory, an ideal PR controller has infinite gain at the fundamental frequency resulting in zero steady-state error. The practical implementation resulted in an average steady-state error of 0.127% among the tests.

6.5. Comparison of PID and PR Control

It was found that both control methods were suitable for output voltage regulation, but each controller had its best and worst features. The following is a summary of the overall results:

- During open-loop operation the output voltage decreases from the 230 V reference to as low as 206V when a 300W load is applied corresponding to a 10.43% voltage drop.
- PID control: Across multiple tests with valid steady-state results, the average voltage error is approximately 0.152%, with an average overshoot of 1.039%.
- PR control: Across multiple tests with valid steady-state results, the average voltage error is lower at approximately 0.127%, but the average overshoot is higher than PID, at 3.09%.
- The main finding was that both controllers can regulate the steady-state voltage close to 230 V, but results show that PID provides slightly better transient behaviour and less overshoot, while PR can achieve slightly better steady-state accuracy.
- It was also found that even with a derivate filter implemented, PI configurations outperformed PID configurations because higher derivative gains caused erratic error corrections and oscillations.
- Using these results, I chose a PI controller configuration for the final inverter design as it had a good balance of responsiveness, accuracy, disturbance rejection and stability.
- Keep in mind that these results should not be taken as definitive evidence that PID/PI control is inherently superior to PR control. The two controllers used different feedback circuits, signal conditioning, calibration and sampling frequencies, so it is not a completely fair comparison.

6.6. Output Filter Results

A number of tests were done where both the filter inductance and filter capacitance were varied to find out how the filter design affects overall performance. For all tests the procedure started with an idle current measurement (no-load) and then the rest of the measurements including THD were done with a 350W resistive load.

An interesting finding was that the idle current of the inverter decreased with an increase in series inductance. Idle current is an extremely important performance parameter in inverters as a high no load power draw will cause the battery bank to be drained just because the inverter is on. So why would the idle current decrease as the choke inductance increases? Well, we know that as series inductance increases the impedance increases for higher frequency current. Therefore, my assumption is that the transformer is better isolated from the high frequency components of the 20kHz PWM.

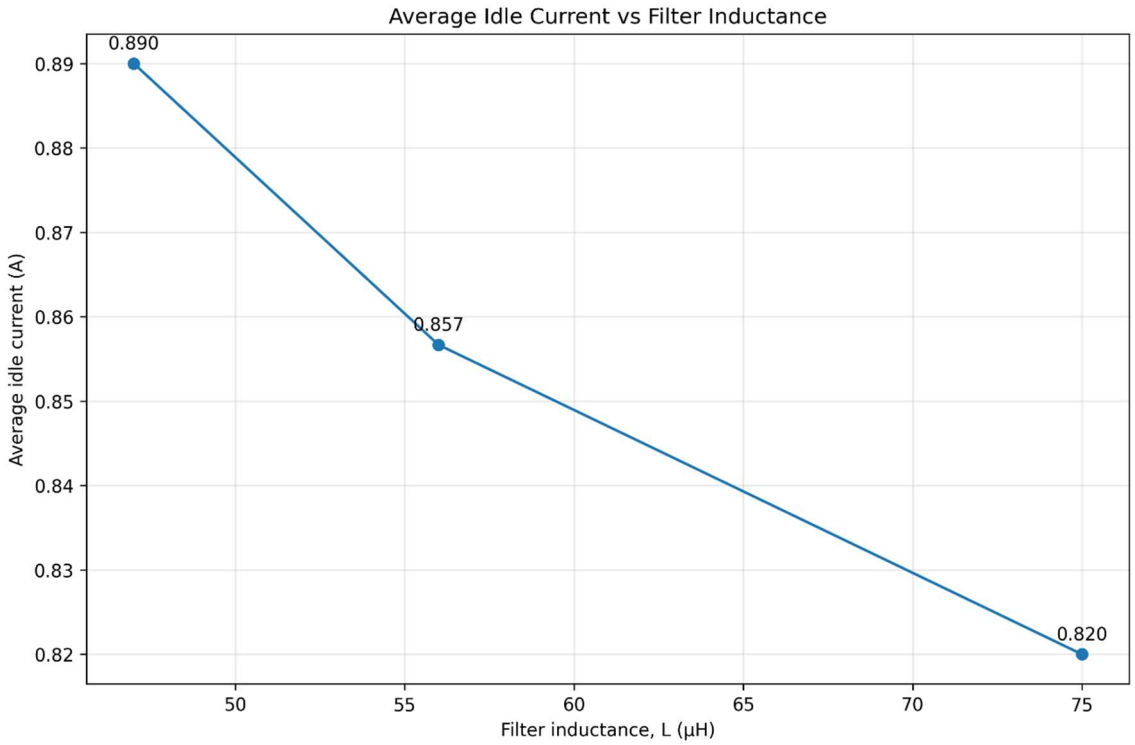


Figure 44: Idle current vs filter inductance

The results obtained also showed a decrease in THD as the filter inductance and capacitance were increased, but after a certain point an increase in filter size led to diminishing performance improvements. These findings were expected as shifting the filter cutoff frequency closer towards the 50Hz fundamental meant that more high frequency harmonics would be attenuated. It was also noted that there were no meaningful changes in inverter efficiency as the filter was changed.

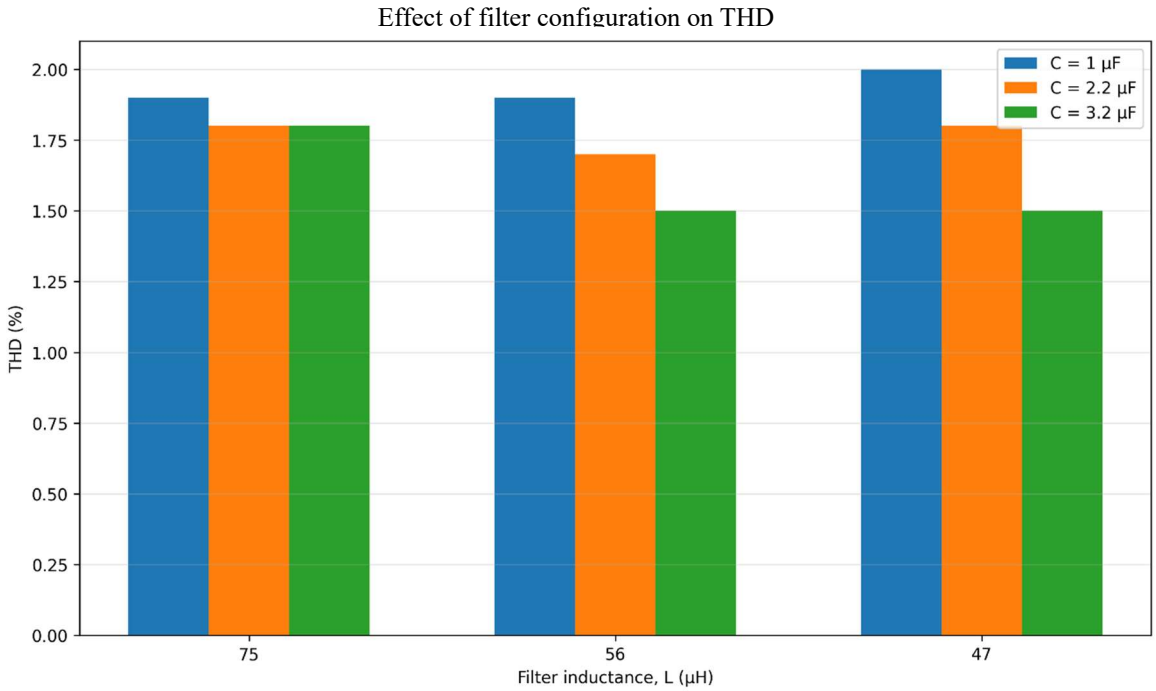


Figure 45: Filter configuration vs THD

L (uH)	C (uF)	Vin (V)	Iin (A)	Vout (V)	Iout (A)	Efficiency (%)	THD (%)	Idle current (A)
75	3.2	26.2	16.07	230	1.54	84.126	1.8	0.81
56	3.2	26.2	16.02	231	1.53	84.205	1.5	0.83
47	3.2	26.2	16.04	231	1.54	84.650	1.5	0.86
75	2.2	26.2	16.03	230	1.53	83.789	1.8	0.81
56	2.2	26.2	16.04	231	1.53	84.100	1.7	0.84
47	2.2	26.2	16.04	230	1.55	84.831	1.8	0.87
75	1	26.1	16.04	231	1.54	84.974	1.9	0.84
56	1	26.1	16.08	230	1.54	84.396	1.9	0.9
47	1	26.1	16.1	231	1.54	84.658	2	0.94

Table 9: Filter configuration and performance parameters

The scope screenshot in figure 46 below shows a slight bit of visible waveform distortion at the zero crossing. This occurred when the filter inductance and capacitance were at the lowest values (47uH and 1uF). The THD reading for this test came out as 2% and the idle current was also at a highest value of 0.94A. The battery bank at this time was sitting at around 26.1V meaning that the no-load power consumption of the inverter was as high as 24.53W.

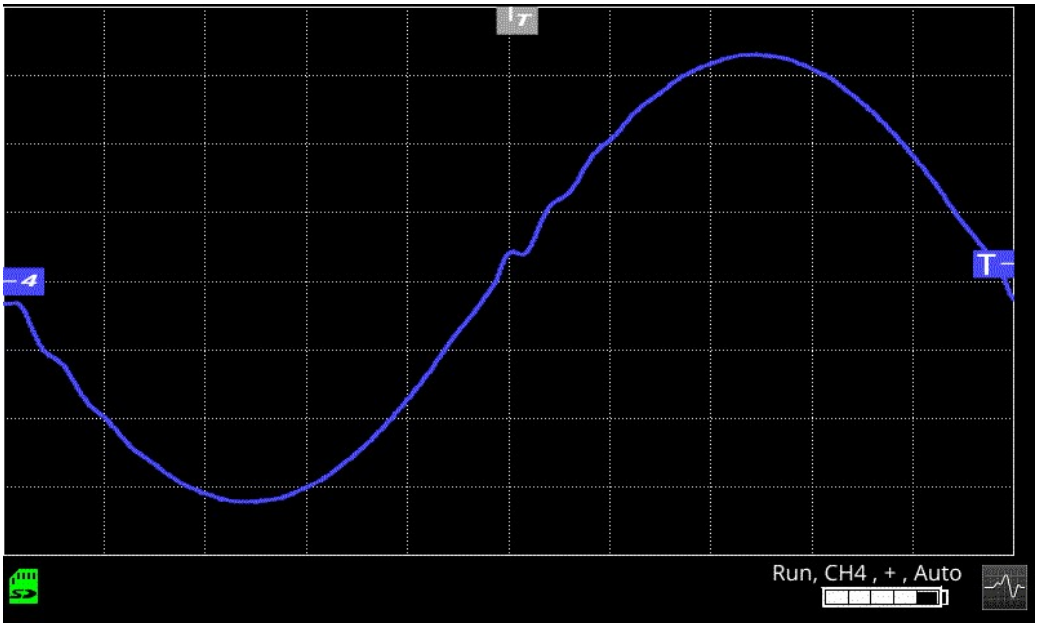


Figure 46: Waveform distortion at the zero crossing (47uH and 1uF)

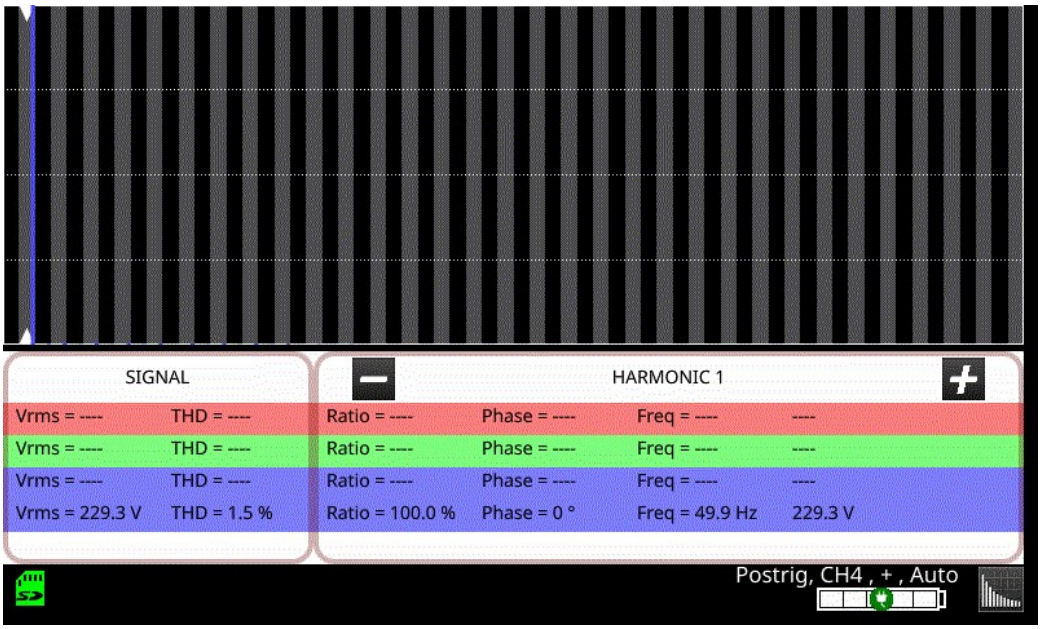


Figure 47: Best THD reading (56uH and 3.2uF)

6.7. Final Optimized Design

Once all testing was completed and research questions were answered, the final design was developed. The system utilized the best performing PWM strategy, control method, controller gains and LC filter configuration. Both the design parameters and achieved specifications can be seen in the tables below.

Design parameter	**Value**
Topology	Full bridge and toroidal transformer
PWM strategy	Fast-slow leg unipolar PWM
Switching frequency	20kHz
Control method	PI (PID structure but Kd = 0)
LC Filter	L = 56uH, C = 3.2uF
Cooling	Temperature controlled fan and heatsinks
Overload protection	63A DC circuit breaker
Start-up	2.5s soft start

Table 10: Final design parameters

Achieved specifications	**Value**
Input voltage	22-28V DC
Output voltage	230V AC ±5% (SANS standard is ±10%)
Output frequency	50Hz ±0.2% (NERSA standard is ±2%)
Power rating	1kVA (Not confirmed if continuous)
Waveform type	Pure sine wave
THD	Less than 2% (Resistive loads)
Efficiency	Greater than 84% (400W load and above)
Idle power draw	~21.75W

Table 11: Achieved specifications

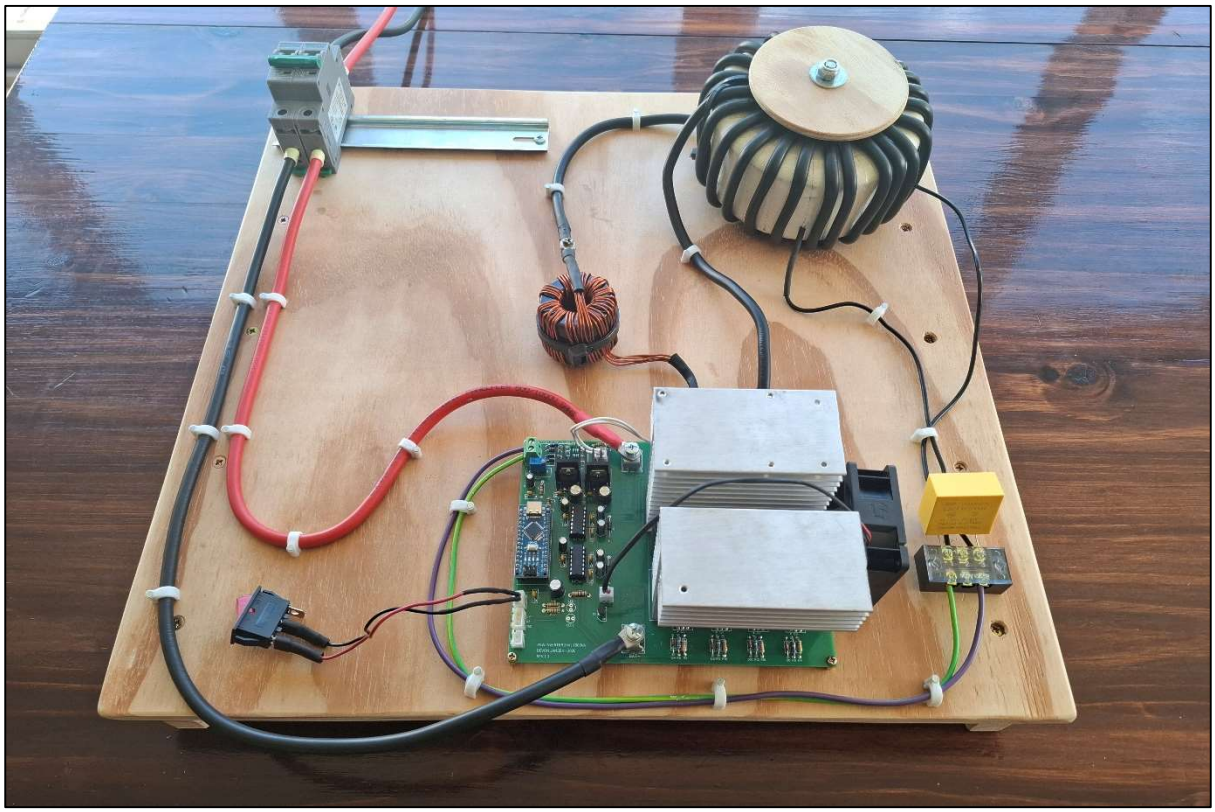


Figure 48: Complete experimental design

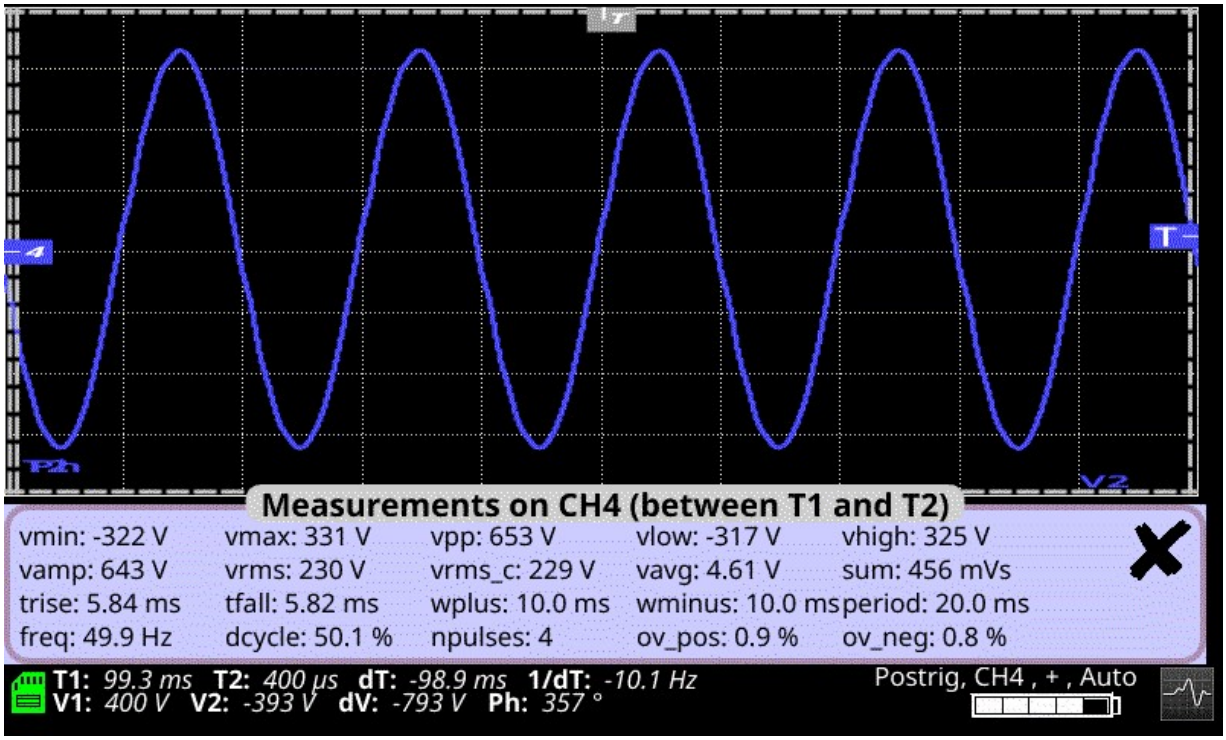


Figure 49: Output waveform of optimized design

7. Conclusion and Recommendations

7.1. Conclusion

The primary aim of this project was to design and optimize a 1kVA single-phase inverter, with a focus on output voltage regulation, harmonic distortion and efficiency. This was done through the practical implementation of a transformer-based inverter using a full-bridge topology, fast-slow leg unipolar PWM, closed-loop control and an LC filter. Both simulation and experimental testing was used to compare the different configurations and measure performance.

Simulations were initially used to find the best performing PWM strategy and experiment with both PID and PR control before practical implementation. The results showed that fast-slow leg unipolar PWM outperformed bipolar PWM and was therefore selected for the inverter design at a switching frequency of 20kHz. It was also found that bipolar PWM required a second choke whereas unipolar PWM only required one choke to attenuate the high frequency switching at the H-bridge output. After simulation results were obtained, an experimental prototype was built.

The first experimental testing was done using open-loop operation and the results emphasized how important closed-loop voltage regulation was. During open-loop operation, the inverter output voltage would keep dropping as the load was increased with the output voltage dropping from 230V down to 206V with a 300W resistive load. After the implementation of both PID and PR control, it was found that both control methods were suitable for output voltage regulation with a significant increase in steady-state performance. Multiple tests were done where the PID and PR controllers achieved average steady-state errors of around 0.152% and 0.127% respectively.

Although the PR controller showed a slightly better average steady-state error, the PID controller showed better transient performance on average. The PID controller outperformed PR control in overshoot, undershoot and settling time after a load disturbance was introduced. The PR controller was also more sensitive to changes in controller gains where some tests showed a higher proportional and resonant gain caused oscillations and instability. The PID controller also became unstable when the derivative gain was increased too much, which led to the finding that a PI configuration would often outperform PID. In literature, PR controllers are more commonly used for current control loops of grid-tied inverters whereas PI controllers are the standard for off-grid inverter applications. In these experiments both controllers used two different feedback signals and circuits, so we cannot use these results to conclude that one control method is definitely better than the other.

Experimentation with LC filter configurations for the transformer-based inverter found that the best arrangement was to have the series inductor on the transformer primary and the parallel capacitor on the secondary. Increasing the filter inductance generally decreased the idle current of the inverter, indicating that the high frequency switching is better isolated from the transformer primary. Increasing both filter inductance and capacitance resulted in lower THD readings with diminishing returns after a certain point. One filter configuration using 56uH and 3.2uF achieved a THD as low as 1.5% under a resistive load. These tests proved that there is a fine balance between achieving good harmonic reduction, lower idle power consumption and practical component selection.

Overall, the project achieved its main objective of designing a 1kVA single-phase inverter and investigated the proposed research questions. The inverter achieved good steady-state voltage regulation, low harmonic distortion and a decent peak efficiency for a prototype. Based on the test results, a PI controller was selected for the final optimized design because of its better transient performance and stability. Further testing is required to confirm whether the inverter is capable of 1kVA continuous output power for an extended period of time.

7.2. Recommendations and future work

The developed inverter prototype and experimental testing showed promising results, but there are some improvements to be made. First, additional stress testing should be done to find out the continuous power and thermal capabilities of the inverter with a 1000VA load. A focus should be placed on the temperature rise of the MOSFETs, choke and transformer over an extended period of time.

Secondly, the controller comparison could be improved upon by testing both PID and PR control using a wider variety of operating conditions and load types. The controllers could not be properly compared if you consider the differences in feedback circuits, signal conditioning, calibration, sampling rates etc. The PR controller settings including resonant bandwidth and phase matching of the feedback signal to the reference could be improved upon. Once these improvements are made, the test results comparing the two controllers may change entirely.

Future research could include current sensing control loops and the implementation of battery charging from the grid making the inverter bidirectional. More protection features could be implemented and further research into reducing transformer losses would increase the overall efficiency of the system. These improvements would result in a more robust system that is suitable for practical standalone applications.

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